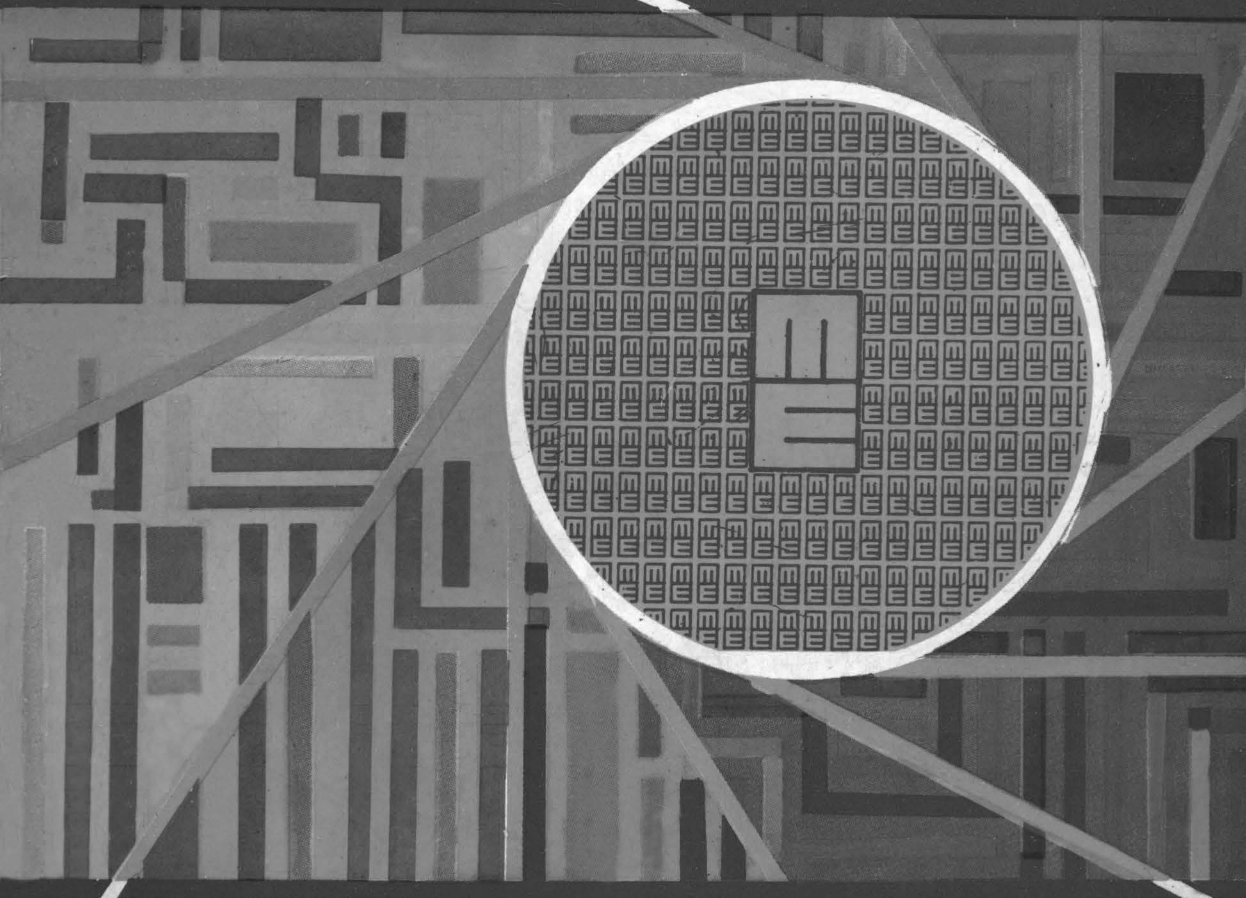
microelectronica



DATA BOOK

DATA BOOK

MOS AND OPTOELECTRONIC DEVICES

FIRST EDITION — 1985

INTRODUCTION

This catalog contains data sheets on MICROELECTRONICA range of MOS integrated circuits and OPTOELECTRONIC devices. Additional information can be obtained by contacting Product Marketing Department.

TABLE OF CONTENTS

microelectronica

34B, Erou Iancu Nicolae Street, 72996 Bucharest, ROMANIA Phone: 33.40.50/504, 549, 565; Telex: 10457 merom r

PRODUCT INDEX

TYPE	FAMILY	DESCRIPTION	PAGE
MDE 2101R	DISPLAY	0.3 inch red seven segment display right hand or left hand decimal point common anode	310
2R	DISPLAY		
3R	DISPLAY		
4R	DISPLAY		
MDE 2101V	DISPLAY	0.3 inch green seven segment display right hand or left hand decimal point common anode	
2V	DISPLAY		
3V	DISPLAY		
4V	DISPLAY		
MDE 2111R	DISPLAY	0.3 inch red seven segment display right hand or left hand decimal point common cathode	314
2R	DISPLAY		
3R	DISPLAY		
4R	DISPLAY		
MDE 2111V	DISPLAY	0.3 inch green seven segment display right hand or left hand decimal point common cathode	314
2V	DISPLAY		
3V	DISPLAY		
4V	DISPLAY		
MDE 2201R	DISPLAY	0.3 inch red overflow indicator right hand or left hand decimal point common anode	318
2R	DISPLAY		
3R	DISPLAY		
4R	DISPLAY		
MDE 2201V	DISPLAY	0.3 inch green overflow indicator right hand or left hand decimal point common anode	318
2V	DISPLAY		
3V	DISPLAY		
4V	DISPLAY		
MDE 2211R	DISPLAY	0.3 inch red overflow indicator right hand or left hand decimal point common cathode	322
2R	DISPLAY		
3R	DISPLAY		
4R	DISPLAY		
MDE 2211V	DISPLAY	0.3 inch green overflow indicator right hand or left hand decimal point common cathode	322
2V	DISPLAY		
3V	DISPLAY		
4V	DISPLAY		
MDE 2573R	DISPLAY	0.3 inch 4 digits red LED numeric display	
4R	DISPLAY		
MDE 2573V	DISPLAY	0.3 inch 4 digits green LED numeric display	326
4V	DISPLAY		
MDE 2583 R	DISPLAY	0.3 inch 4 digits red LED numeric display	328
4 R	DISPLAY		
MDE 2583 V	DISPLAY	0.3 inch 4 digits green LED numeric display	
4V	DISPLAY		
MDE 2911 R	LED	Light indicator with discret LED s (bar graph display)	330
2R	LED		
MDE 2911P	LED		
2P	LED		
MDE 2911G	LED		
2G	LED		
MDE 2911V	LED		
2V	LED		

* Not recommended for new design
• Product in development

GENERAL OPERATING AND HANDLING CONSIDERATIONS

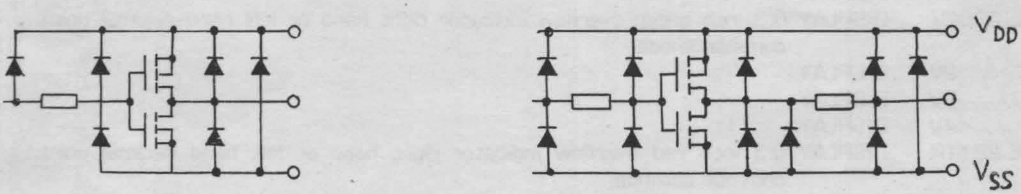
Power - Source Rules

1. The power — supply polarity for CMOS circuits should not be reversed.
   The positive (V_{DD}) terminal should never be more than 0.5V negative with respect to the negative (V_{SS}) terminal ($V_{DD}—V_{SS}>—0.5V$).
   Reversal of polarities will forward — bias and short the structured and protection diode between V_{DD} and V_{SS}.
2. Power — source current capability should be limited to the minimum value wich will assure good logic operation.
3. Large values of resistors in series with V_{DD} or V_{SS} should be avoided transient turn-on of input protection diodes can result from drops across such resistors during switching.
4. When separate power — supplies are used for the CMOS device and for the device inputs, the device power supply should always be turned on before the independent input signal sources, and the input signals should be turned off before the powersupply is turned off (VSS<VI<VDD as a maximum limit). This rule will prevent ever dissipation and possible damage to the input protection diode when the device power supply is grounded. When the device power supply is an open circuit, violation of this rule can result the undesired circuit operation although device damage should not result; ac inputs can be rectified by inputs can be rectified by input diode to act as a power supply

Input signal rules

1. All CMOS inputs should be terminated. When CMOS inputs are wired to edge card connectors with CMOS drive coming from another DC board, a shunt resistor should be connected to V_{DD} or V_{SS}.
2. When CMOS circuits are driven by TTL logic a pull-up resistors should be connected from the CMOS inputs to 5V.
3. Input rise and fall times for clocked devices must not exceed 15 μs in order to avoid high consumption, false triggering etc. With slower inputs a Schmitt trigger must be employed.

Gate - Oxide Protection Network



ORDERING NUMBERS CMOS 4000 SERIES

MMC 4XXX E — for dual in-line plastic package, intermediate temperature range
MMC 4XXX F — for dual in-line ceramic package, frit seal, intermediate temperature range
MMC 4XXX G — for dual in-line ceramic package, extended temperature range
MMC 4XXX H — for dual in-line ceramic package, frit seal, extended temperature range

NOR GATES: 4000 DUAL 3 INPUT PLUS INVERTER 4001 QUAD 2 INPUT 4002 DUAL 4 INPUT 4025 TRIPLE 3 INPUT

GENERAL DESCRIPTION

These NOR gates are monolithic complementary MOS (CMOS) integrated circuits. The N and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.
The MMC 4000, MMC 4001, MMC 4002 and MMC 4025E/F/G/H
NOR gates provide the system designer with direct implementation of the NOR function.
The MMC 4000, MMC 4001, MMC 4002 and MMC 4025E/F/G/H types are supplied in 14-lead hermetic dual-in-line ceramic or plastic packages

FEATURES

- Propagation delay time = 60 ns (typ) at C_L = 50 pF V_{DD} = 10 V
- Buffered inputs and outputs
- Standardized symmetrical output characteristics
- 100% tested for maximum quiescent current
- 5 V, 10 V and 15 V parametric ratings
- High noise immunity: 0.45 V_{DD} (typical)

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

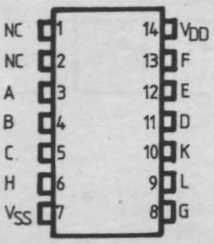
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

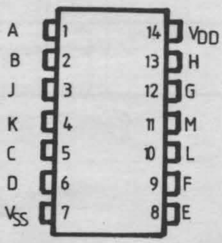
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAMS

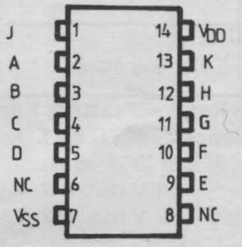
MMC 4000



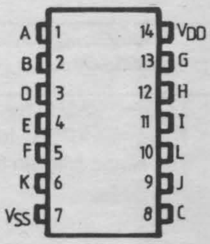
MMC 4001



MMC 4002



MMC 4025



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
		E, F types	0/ 5			5		1		0.01	1		7.5	
			0/10			10		2		0.01	2		15	
			0/15			15		4		0.01	4		30	
V_{OH}	Output high voltage		0/ 5		<1	5	4.95		4.95			4.95		V
			0/10		<1	10	9.95		9.95			9.95		
			0/15		<1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		<1	5		0.05			0.05		0.05	V
			10/0		<1	10		0.05			0.05		0.05	
			15/0		<1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	<1	5	3.5		3.5			3.5		V
				1/9	<1	10	7		7			7		
				1.5/13.5	<1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	<1	5		1.5			1.5		1.5	V
				9/1	<1	10		3			3		3	
				13.5/1.5	<1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V

2 V min. with $V_{DD} = 10$ V

2.5 V min. with $V_{DD} = 15$ V

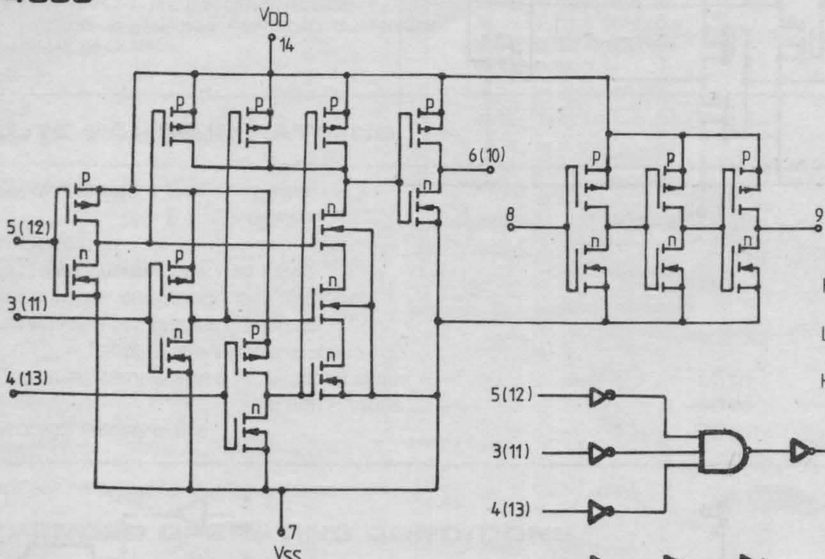
DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200k, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and and fall times = 20 ns)

PARAMETER		TEST CONDITIONS	VALUES			UNIT
		V_{DD} (V)	min	typ	max	
t_{PLH} t_{PHL}	Propagation delay time	5		125	250	ns
		10		60	120	
		15		45	90	
t_{THL} t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	

SCHEMATIC AND LOGIC DIAGRAMS

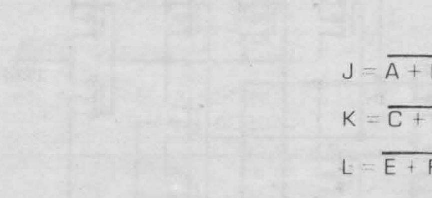
MMC 4000



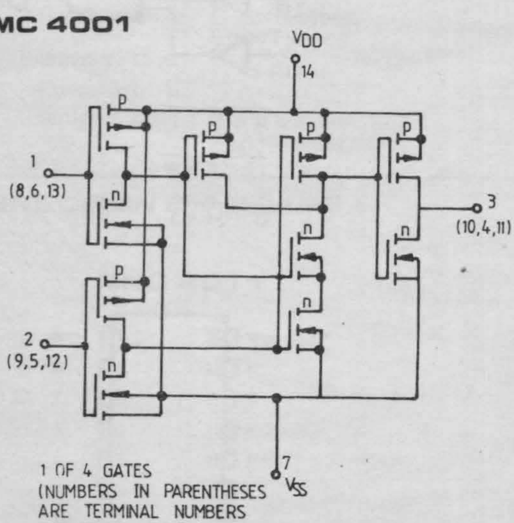
$H = \overline{A + B + C}$

$L = \overline{G}$

$K = \overline{D + E + F}$



MMC 4001



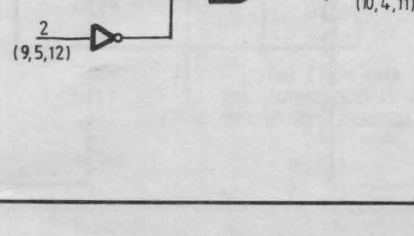
1 OF 4 GATES
(NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR OTHER GATES)

$J = \overline{A + B}$

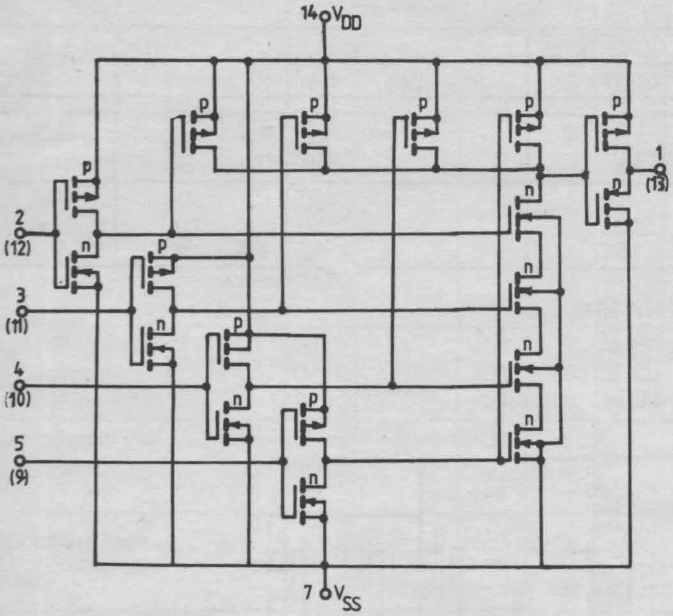
$K = \overline{C + D}$

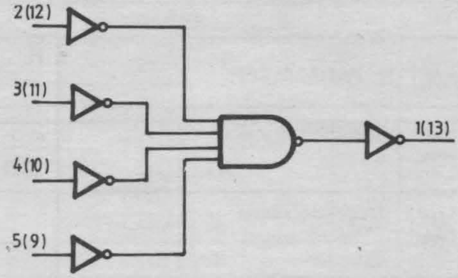
$L = \overline{E + F}$

$M = \overline{G + H}$



MMC 4002

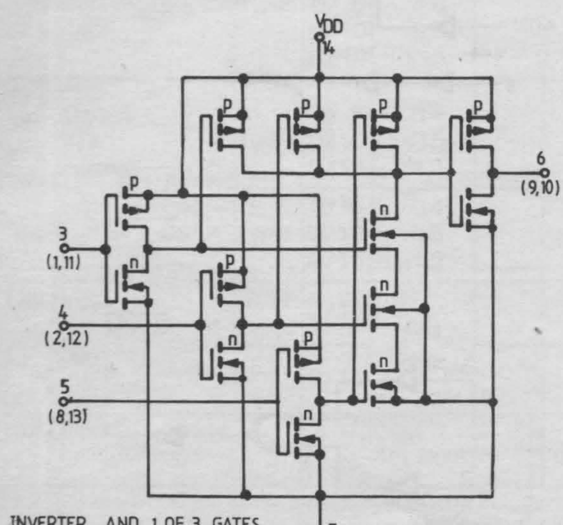




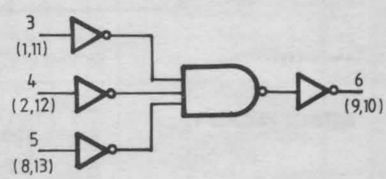
J $\overline{A+B+c+D}$

K $\overline{E+F+G+H}$

MMC 4025



INVERTER AND 1 OF 3 GATES
(NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR SECOND GATE)



$J = \overline{A+B+C}$

$K = \overline{D+E+F}$

$L = \overline{G+H+I}$

NAND GATES: 4011 QUAD 2 INPUT 4012 DUAL 4 INPUT 4023 TRIPLE 3 INPUT

GENERAL DESCRIPTION

These NAND gates are monolithic complementary MOS (CMOS) integrated circuits. The N and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No. DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

The MMC 4011, MMC 4012 and MMC 4023E/F/G/H NAND gates provide the system designer with direct implementation of the NAND function. All inputs and outputs are buffered.

The MMC 4011, MMC 4012 and MMC 4023E/F/G/H types are supplied in 14-lead hermetic dual-in-line ceramic or plastic packages.

FEATURES

- Propagation delay time = 60 ns (typ.) at C_L = 50 pF, V_{DD} = 10 V
- Buffered inputs and outputs
- 5 V, 10 V and 15 V parametric ratings
- 100% tested quiescent current
- High noise immunity 0.45 V_{DD} (typical)

APPLICATIONS

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_i	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		±10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range		100	mW
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltages are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_i	Imput voltage	0 to	V_{DD}	V
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAMS

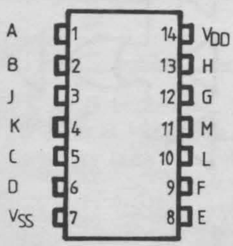
MMC 4011

J = A · B

K = C · D

L = E · F

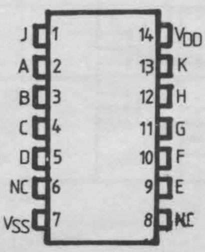
M = G · H



MMC 4012

J = A · B · C · D

K = E · F · G · H

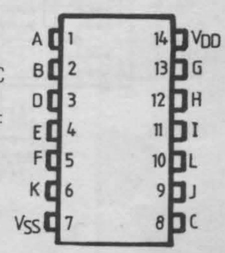


MMC 4023

J = A · B · C

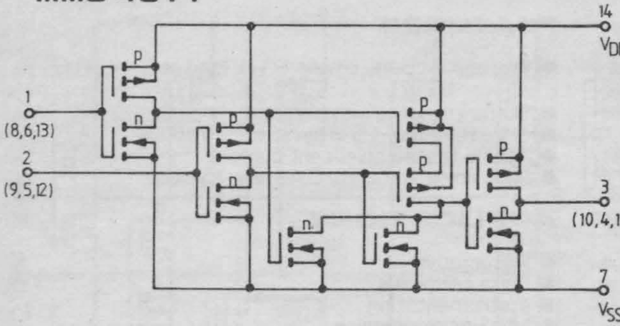
K = D · E · F

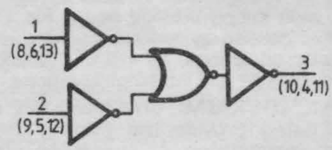
L = G · H · I



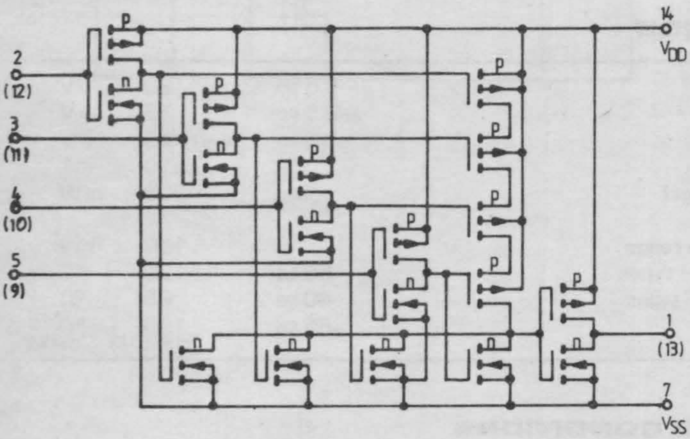
SCHEMATIC AND LOGIC DIAGRAMS

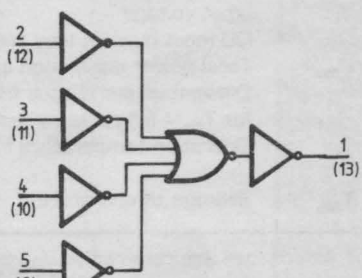
MMC 4011



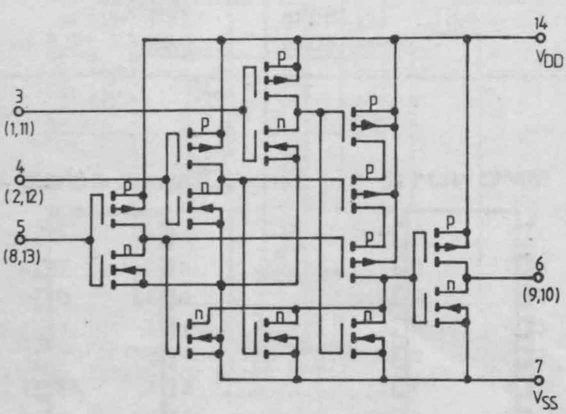


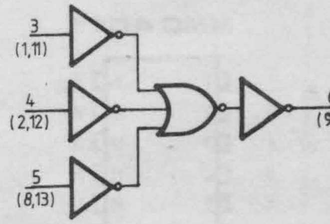
MMC 4012





MMC 4023





STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

Parameter			Test conditions V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	Values T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	Unit
I_L	Quiescent current	G, H types	0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
		E, F types	0/ 5			5		1		0.01	1		7.5	
			0/10			10		2		0.01	2		15	
			0/15			15		4		0.01	4		30	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

PARAMETER		TEST CONDITIONS	VALUES			UNIT
		V_{DD} (V)	min	typ	max	
t_{PLH}, t_{PHL}	Propagation delay time	5		125	250	ns
		10		60	120	
		15		45	90	
t_{THL}, t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	

DUAL "D" - TYPE FLIP-FLOP

GENERAL DESCRIPTION

The MMC 4013 is a monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package.

The MMP 4013 consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and, by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

FEATURES

- set-reset capability
- static flip-flop operation — retains state indefinitely with clock level either "high" or "low"
- medium-speed operation — 16 MHz (typ.) clock toggle rate at 10 V
- quiescent current specified to 20 V
- maximum input leakage of 1 μA at 18 V (full package temperature range)
- standardized symmetrical output characteristics
- 5 V, 10 V, and 15 V parametric ratings

ABSOLUTE MAXIMUM RATINGS

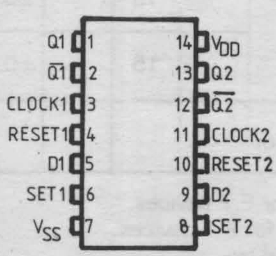
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Imput voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

Symbol	Parameter	Types	V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		<1	5	4.95		4.95			4.95		V
			0/10		<1	10	9.95		9.95			9.95		
			0/15		<1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		<1	5		0.05			0.05		0.05	V
			10/0		<1	10		0.05			0.05		0.05	
			15/0		<1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	<1	5	3.5		3.5			3.5		V
				1/9	<1	10	7		7			7		
				1.5/13.5	<1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	<1	5		1.5			1.5		1.5	V
				9/1	<1	10		3			3		3	
				13.5/1.5	<1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15	Any input		15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kohm, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20 ns)

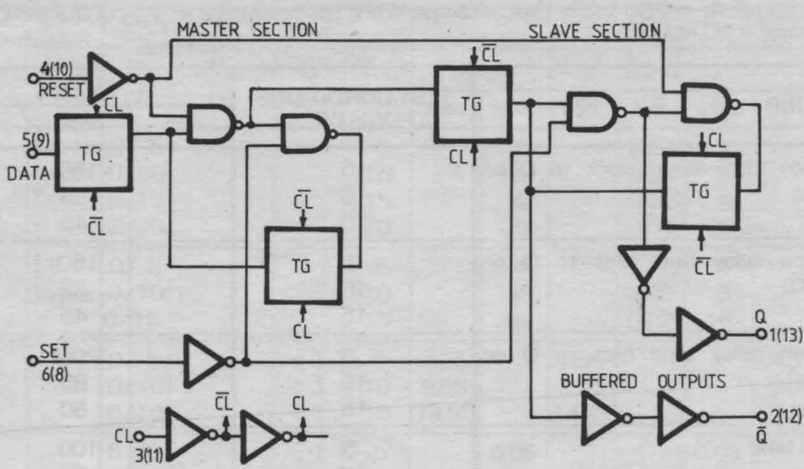
	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES min.	typ.	max.	UNIT
t_{PLH}, t_{PHL}	Propagation delay time (clock to Q or $\bar{Q}$ outputs)	5		150	300	ns
		10		65	130	
		15		45	90	
t_{PLH},	Propagation delay time (Set to Q or Reset to $\bar{Q}$)	5		150	300	ns
		10		65	130	
		15		45	90	
t_{PHL},	Propagation delay time (Set to $\bar{Q}$ or Q outputs)	5		200	400	ns
		10		85	170	
		15		60	120	
t_{TLH}, t_{THL}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
f_{CL}●	Maximum clock frequency	5	3.5	7		MHz
		10	8	16		
		15	12	24		
t_W	Clock pulse width	5	140	70		ns
		10	60	30		
		15	40	20		
t_r, t_f●●	Clock input rise or fall time	5			15	μs
		10			4	
		15			1	
t_W	Set or reset pulse width	5	180	90		ns
		10	80	40		
		15	50	25		
t_{setup}	Data setup time	5	40	20		ns
		10	20	10		
		15	15	7		

● Input t_r, t_f = 5 ns

●● If more than one unit is cascaded in a parallel clocked operation, tr should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

LOGIC DIAGRAM

(one of two identical flip-flops)



N(N) = FF1/FF2 TERMINAL ASSIGNEMENT

TRUTH TABLE

CL●	D	R	S	Q	$\overline{Q}$	
↑	0	0	0	0	1	
↑	1	0	0	1	0	
↓	X	0	0	Q	$\overline{Q}$	NO CHANGE
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

LOGIC 0 = LOW
LOGIC 1 = HIGH

● = LEVEL CHANGE
X = DON'T CARE

8-STAGE STATIC SHIFT REGISTERS: SYNCHRONOUS PARALLEL OR SERIAL INPUT/SERIAL OUTPUT: MMC 4014 ASYNCHRONOUS PARALLEL INPUT OR SYNCHRONOUS SERIAL INPUT/SERIAL OUTPUT: MMC 4021

GENERAL DESCRIPTION

The MMC 4014, MMC 4021 series types are 8-stage parallel-or serial-input/serial-output registers having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL data input, and individual parallel "JAM" inputs to each register stage. Each register stage is a D type, master-slave flip-flop; in addition to an output from stage 8, "Q" outputs are also available from stage 6 and 7..

Parallel as well as serial entry is made into the register synchronously with the positive clock line transition in the MMC 4014. In the MMC 4021 serial entry is synchronous with the clock but parallel entry is asynchronous.

In both types, entry is controlled by the PARALLEL/SERIAL CONTROL input.

When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line.

When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line.

In the MMC 4021, the CLOCK input of the internal stage is "forced" when asynchronous parallel entry is made.

Register expansion using multiple package is permitted.

The MMC 4014, MMC 4021 series types are supplied in 16-lead dual-in-line plastic or ceramic package.

FEATURES

- Medium speed operation-12 MHz (typ.) clock rate. at $V_{DD}—V_{SS} = 10$ V
- Fully static operation
- 8 Master-Slave flip-flops plus output buffering and control gating

ABSOLUTE MAXIMUM RATINGS

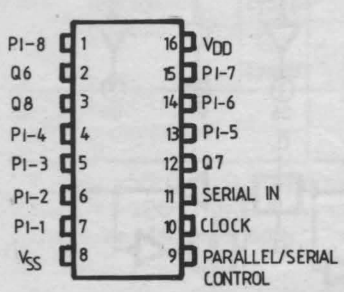
V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_i	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		±10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_i	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



TRUTH TABLE

For 4014

CL	Serial input	Parallel/serial control	P I-1	P I-n	Q_1 (internal)	Q_n	
	X	1	0	0	0	0	
	X	1	1	0	1	0	
	X	1	0	1	0	1	
	X	1	1	1	1	1	
	0	0	X	X	0	Q_n-1	
	1	0	X	X	1	Q_n-1	
	X	X	X	X	Q_1	Q_n	NC

X = Don't care case NC = No change

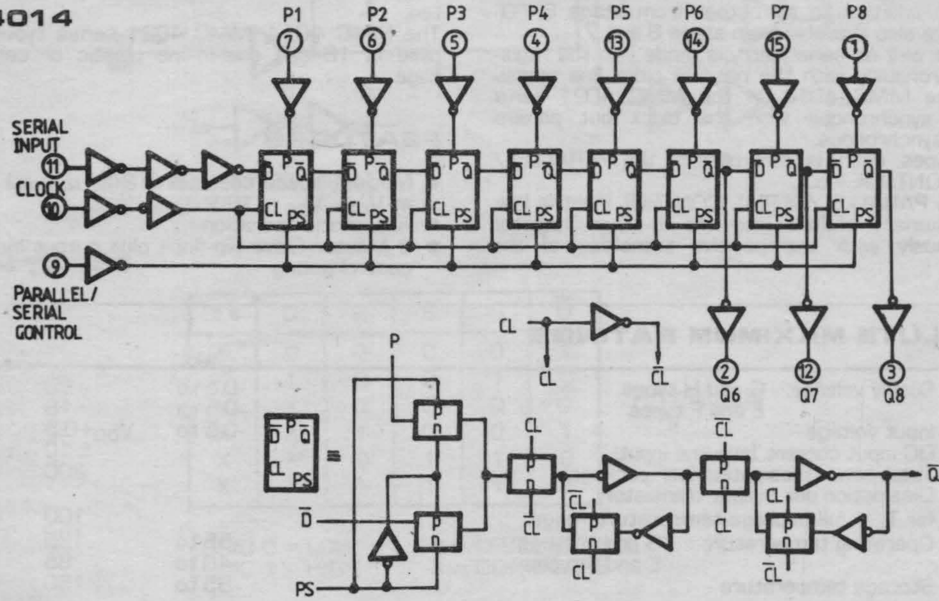
LOGIC DIAGRAMS AND TRUTH TABLE

For MMC 4021

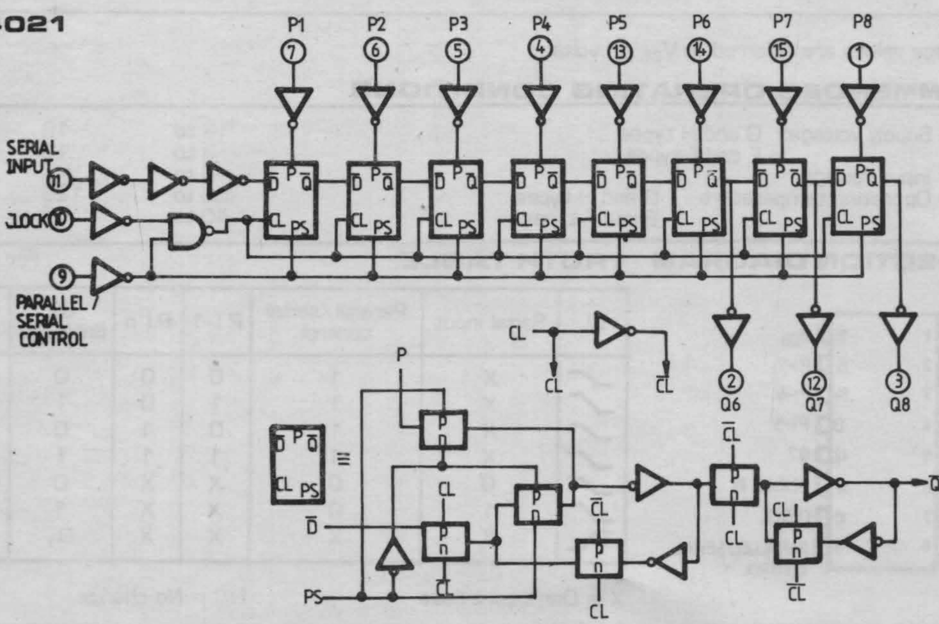
CL	Serial input	Parallel/serial control	P I-1	P I-n	Q_1 (internal)	Q_n	
X	X	1	0	0	0	0	
X	X	1	0	1	0	1	
X	X	1	1	0	1	0	
X	X	1	1	1	1	1	
	0	0	X	X	0	Q_{n-1}	
	1	0	X	X	1	Q_{n-1}	
	X	0	X	X	Q_1	Q_n	NC

X = Don't care case NC = No change

MMC 4014



MMC 4021



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kohm, typical temperature coefficient for all $V_{DD} = 0.3\%/°C$ values, all input rise and fall times= 20 ns)

PARAMETER		TEST CONDITIONS		VALUES			UNIT
			V_{DD} (V)	min.	typ.	max.	
Clocked operation							
t_{PLH}, t_{PHL}	Propagation delay time		5 10 15		160 80 60	320 160 120	ns
t_{THL}, t_{TLH}	Transition time		5 10 15		100 50 40	200 100 80	ns
f_{CL}*	Maximum clock input frequency		5 10 15	3 6 8.5	6 12 17		MHz
t_W	Clock pulse width		5 10 15	180 80 50	90 40 25		ns
t_r, t_f	Clock input rise or fall time		5 10 15			15 15 15	µs
t_{setup}	Setup time, serial input (ref. to CL)		5 10 15	120 80 60	60 40 30		ns
t_{setup}	Setup time, paralel inputs (4014) (ref. to CL)		5 10 15	80 50 40	40 25 20		ns
t_{setup}	Setup time, paralllel inputs (4021)		5 10 15	50 30 20	25 15 10		ns
t_{setup}	Setup time, parallel/serial control (4014) (ref. to CL)		5 10 15	180 80 60	90 40 30		ns
t_{hold}	Hold time, serial in, parallel in, parallel/serial control		5 10 15	0 0 0			ns
t_{WH}	P/S Pulse width (4021)		5 10 15	160 80 50	80 40 25		ns
t_{rem}	P/S Removal, time (4021) (ref. to CL)		5 10 15	280 140 100	140 70 50		ns

* If more then one unit is cascated t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

DUAL 4-STAGE STATIC SHIFT REGISTER WITH SERIAL INPUT/PARALLEL OUTPUT

GENERAL DESCRIPTION

The MMC 4015 (G and H types) and MMC 4015 (E and F types) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package.

The MMC 4015 consists of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent CLOCK and RESET inputs as well as a single serial DATA input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the DATA inputs is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one MMC 4015 package, or to more than 8 stages using additional MMC 4015's is possible.

FEATURES

- Medium speed operation: 12 MHz (typ.) clock rate at $V_{DD}—V_{SS} = 10$ V.
- Fully static operation.
- 8 master-slave flip-flops plus input and output buffering
- High noise immunity

ABSOLUTE MAXIMUM RATINGS

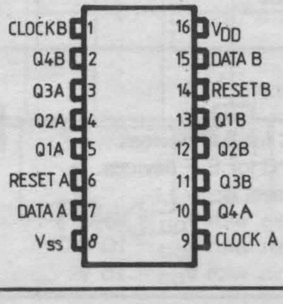
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			± 10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V

2 V min. with $V_{DD} = 10$ V

2.5 V min. with $V_{DD} = 15$ V

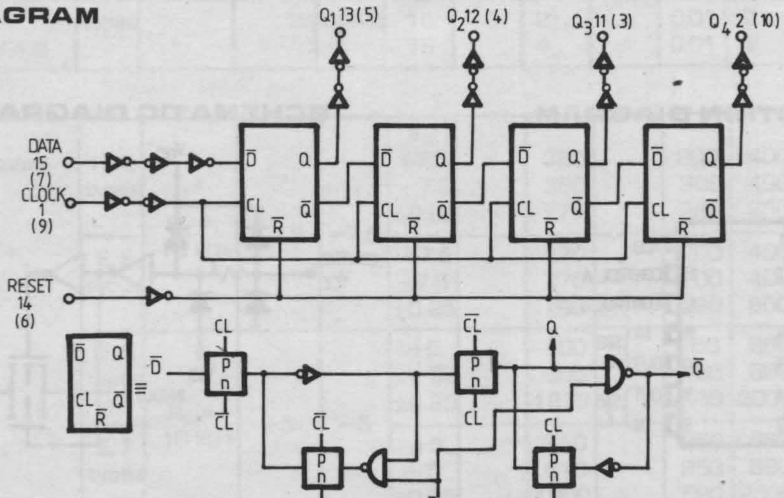
DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times= 20 ns)

	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES min.	VALUES typ.	VALUES max.	UNIT
Clocked operation						
t_{PLH}, t_{PHL}	Propagation delay time (Carry Out or Decoded out Lines)	5 10 15		160 80 60	320 160 120	ns
t_{THL}, t_{TLH}	Transition time (Carry Out or Decoded Out Lines)	5 10 15		100 50 40	200 100 80	ns
f_{CL}	Maximum clock input frequency	5 10 15	3 6 8.5	6 12 17		MHz
t_W,	Clock pulse width	5 10 15	180 80 50	90 40 25		ns
t_r, t_f※	Clock input rise or fall time	5 10 15			15 15 15	μs
t_{setup}	Data setup time	5 10 15	70 40 30	35 20 15		ns
Reset operation						
t_{PLH}, t_{PHL}	Propagation delay time	5 10 15		200 100 80	400 200 160	ns
t_W,	Reset pulse width	5 10 15	200 80 60	100 40 30		ns

※ If more than one unit is cascaded t_r CL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

LOGIC DIAGRAM



QUAD BILATERAL SWITCH

GENERAL DESCRIPTION

The MMC 4016 (intermediate or extended temperature range) are monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package.
The MMC 4016 types are quad bilateral switches intended for the transmission or multiplexing of analog or digital signals. Each of the four independent bilateral switches has a single control signal input which simultaneously biases both the p and n device in a given switch ON or OFF.

FEATURES

- 20 V digital or ± 10 V peak-to-peak switching
- 280 ohm typical ON resistance for 15 V operation
- Switch on resistance matched to within 10 ohm typ. over 15 V signal input range
- Extremely high control input impedance (control circuit isolated from signal circuit 10^{12} ohm typ.)
- Extremely low off switch leakage resulting in very low offset current and high effective off resistance: 110 pA typ. $V_{DD}-V_{SS}$ = 18 V, T_A = 25°C
- Matched control-input to signal-output capacitance: reduces output signal transients.
- Frequency response switch on = 40 MHz (typ.).

ABSOLUTE MAXIMUM RATINGS

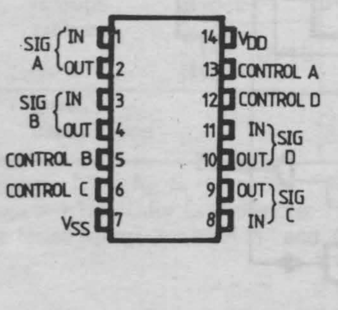
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			± 10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

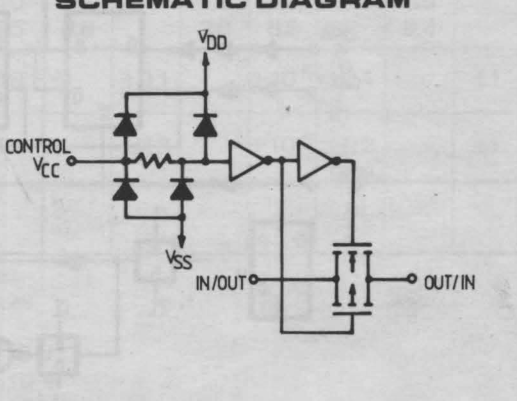
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



SCHEMATIC DIAGRAM



TYPICAL „ON" RESISTANCE CHARACTERISTICS,

$T_A = 25°C$.

CHARACTERISTIC*	SUPPLY CONDITIONS		LOAD CONDITIONS					
			$R_L = 1\ k\Omega$		$R_L = 10\ k\Omega$		$R_L = 100\ k\Omega$	
	V_{DD} (V)	V_{SS} (V)	VALUE (Ω)	V_{IS} (V)	VALUE (Ω)	V_{IS} (V)	VALUE (Ω)	V_{IS} (V)
R_{ON}	+15	0	200 200	+15 0	200 200	+15 0	180 200	+15 0
R_{ON} (max.)	+15	0	300	+11	300	+9.3	320	+9.2
R_{ON}	+10	0	290 290	+10 0	250 250	+10 0	240 300	+10 0
R_{ON} (max.)	+10	0	500	+7.4	560	+5.6	610	+5.5
R_{ON}	+5	0	860 600	+5 0	470 580	+5 0	450 800	+5 0
R_{ON} (max.)	+5	0	1.7 k	+4.2	7k	+2.9	33 k	+2.7
R_{ON}	+2.5	−2.5	590 720	+2.5 −2.5	450 520	+2.5 −2.5	490 520	+2.5 −2.5
R_{ON} (max.)	+2.5	−2.5	232 k	± 0.25	300 k	± 0.25	870 k	± 0.25

* Variation from a perfect switch, $R_{ON} = 0\ \Omega$

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS				VALUES							UNIT
			$V_C = V_{DD}$	V_{SS} (V)	V_{DD} (V)	T_{LOW}		25°C			T_{HIGH}		
						min.	max.	min.	typ	max.	min.	max.	
I_L Quiescent device current (all switches ON or all switches OFF)	G, H types				5		0.25		0.01	0.25		7.5	μA
					10		0.5		0.01	0.5		15	
					15		1		0.01	1		30	
					20		5		0.02	5		150	
	E, F types				5		1		0.01	1		7.5	
					10		2		0.01	2		15	
					15		4		0.01	4		30	
Switch													
					V_{IS}								
R_{ON} ON Resistance	H, G types	$R_L =$ 10 kΩ•	+7.5	−7.5	+7.5		360		200	400		600	Ω
					−7.5		360		200	400		600	
					±0.25		775		280	850		1230	
	E, F types				+7.5		370		200	400		520	
					−7.5		370		200	400		520	
					+0.25		790		280	850		1080	
	H, G types	$R_L =$ 10 kΩ•	+5	−5	+5		600		250	660		960	Ω
					−5		600		250	660		960	
					±0.25		1870		580	2000		2600	
	E, F types				+5		610		250	660		840	
					−5		610		250	660		840	
					±0.25		1900		580	2000		2380	

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS	$V_C = V_{DD}$	V_{SS} (V)	V_{DD} (V)	T_{LOW} min.	T_{LOW} max.	25°C min.	25°C typ	25°C max.	T_{HIGH} min.	T_{HIGH} max.	UNIT
	G, H types	$R_L =$ 10 kΩ●	+15	0	+15		360		200	400		600	Ω
					+0.25		360		200	400		600	
					+9.3		775		300	850		1230	
	E, F types		+15	0	+15		370		200	400		520	
					+0.25		370		200	400		520	
					+9.3		790		300	800		1080	
	G, H types	$R_L =$ 10 kΩ●	+10	0	+10		600		250	660		960	Ω
					+0.25		600		250	660		960	
					+5.6		1870		560	2000		2600	
	E, F types		+10	0	+10		610		250	660		840	
					+0.25		610		250	660		840	
					+5.6		1900		560	2000		2380	
ΔON Resistance (between any 2 of 4 switches)		$R_L =$ 10 kΩ●	+7.5	−7.5	±7.5				10				Ω
			+5	−5	±5				15				
Input or output leakage current switch OFF (effective OFF resistance)	G, H types		V_{DD} +18	$V_C = V_{SS}$ 0			±0.1		10^{-5}	±0.1		1	µA
	E, F types		V_{DD} +15	$V_C = V_{SS}$ 0			±0.3		10^{-5}	±0.3		1	
C_I Input capacitance		$V_{CC} = V_{SS} = -5$			+5				4				pF
C_O Output capacitance									4				
C_{IO} Feedthrough									0.2				
Control (V_C)													
V_{TH} Switch threshold voltage		$I_{IS} = 10\ \mu A$			5	1		1	2.25		1		V
					10	2		2	4.5		2		
					15	2		2	6.75		2		
I_I Input current	G, H types	$V_{IS} \leq V_{DD}$			18		±0.1		$\pm 10^{-5}$	±0.1		±1	µA
	E, F types				15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I Input capacitance									5	7.5			pF

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF all input square wave rise and fall time = 20 ns).

PARAMETER	V_C (V)	TEST CONDITIONS					VALUES			UNIT
		R_L (kΩ)	f_i (KHz.)	V_I (V)	V_{SS} (V)	V_{DD} (V)		typ.	max.	
Switch										
t_{pd} Propagation delay time (Signal input to output)	$= V_{DD}$	10		10 sq. Wave	GND	5 10 15	-	40 20 15	100 50 40	ns
Crosstalk between any 2 of 4 switches (f −50 dB) 20 log $\frac{V_O}{V_I}$ = = −50 dB	$V_{C(A)} = V_{DD} = +5$ $V_{C(B)} = V_{SS} = -5$	1		$V_{I(A)}$ ▲ =5pp				0.9		MHz
Frequency response switch "ON" (Sine wave input) at 20 log $\frac{V_O}{V_I}$ = = −3 dB	$= V_{DD}$ ● = +5	1		5p−p	−5			40		MHz
Feedthrough (Switch) OFF) at 20 log $\frac{V_O}{V_I}$ = −50 dB	$= V_{SS}$ = −5	1		−5p-p		5		1.25		MHz
Sine wave distortion	$= V_{DD}$ = 5	10	1	5p−p	−5			0.4		%
Control (V_C)										
Propagation delay: (Turn ON control to output)	$V_{DD} - V_{SS}$ (Sq. wave)	1		V_{DD} or V_{SS}		5 10 15	$V_{DD}-V_{SS}$ = 10 V	35 20 15	70 40 30	ns
Max. allowable control input repetion rate	10 (Sq. wave)	1		V_{DD}	GND	10		10		MHz
Crosstalk (Control input to signal output)	10(Sq. wave)	10			GND	10		50		mV

(▲) Symetrical about OV
(●) Fir all test conditions.

COUNTER/DIVIDERS: 4017 DECADE COUNTER WITH 10 DECODED OUTPUTS 4022 OCTAL COUNTER WITH 8 DECODED OUTPUTS

GENERAL DESCRIPTION

The MMC 4017 and MMC 4022 are 5-stage and 4 stage Johnson counters having 10 and 8 decoded outputs respectively.
The MMC 4017 and MMC 4022 are monolithic integrated circuits, fabricated in standard Al-gate CMOS technology. Are available in 16-lead dual in-line- plastic package.
Inputs include a CLOCK, a RESET and a CLOCK inhibit signal. Schmitt trigger in the CLOCK input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times. These counters are advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. A high RESET signal clears the counter to its zero count. Use of the Johnson decade-counter configuration permits high-speed operation. 2-input decimal-decode gating and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded Output remains high for one full clok cycle. A CARRY-OUT signal completes one cycle every 10 clock input cycles in the MMC 4017 or every 8 clock input cycles in the MMC 4022 and is used to ripple-clock the succeding device in a multi-device counting chain.

FEATURES

- Fully static operation
- Medium speed operation −12 MHz (typ) at V_{DD} = 10 V

APPLICATIONS

- Decade counter/decimal decode display
- Binary counter/decoder
- Frequency division
- Counter control/timers
- Divide — by — N counting.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	$V_{DD}+0.5$	V
I_I	DC input current (any one input)			± 10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

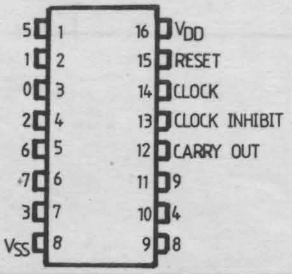
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

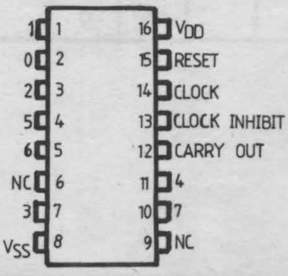
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAMS

MMC 4017

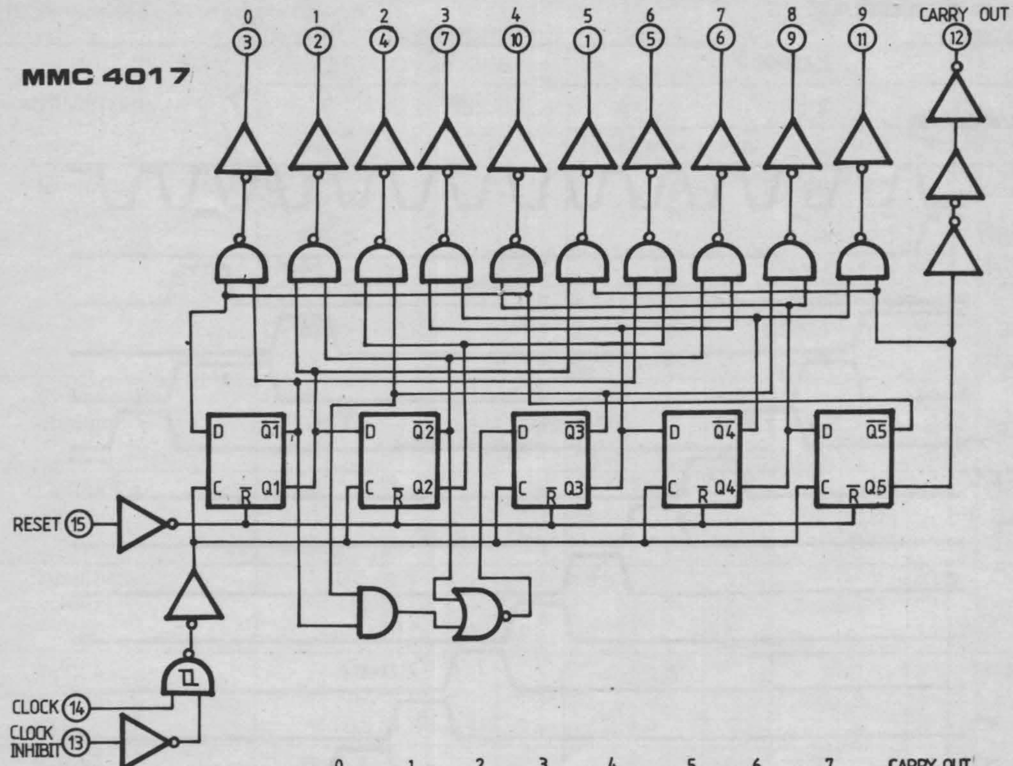


MMC 4022

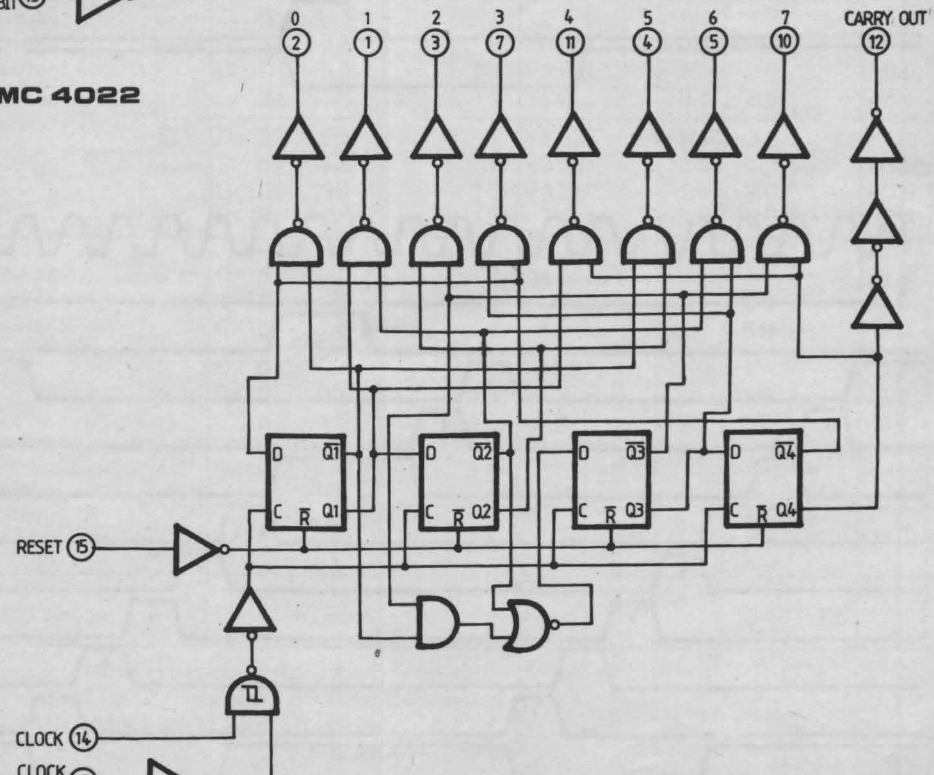


LOGIC DIAGRAM

MMC 4017

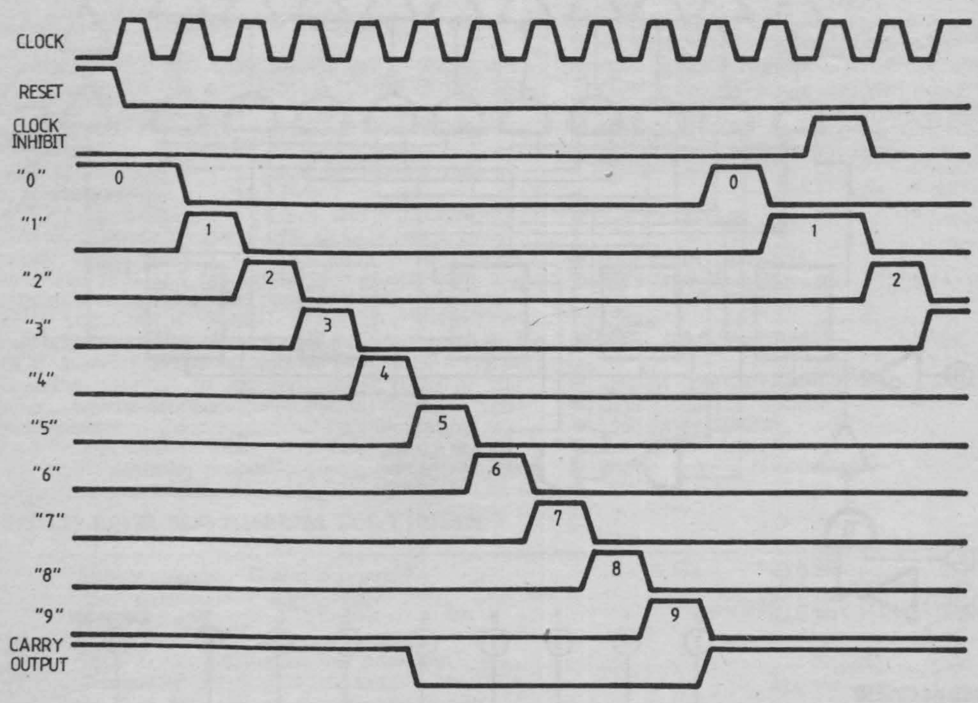


MMC 4022

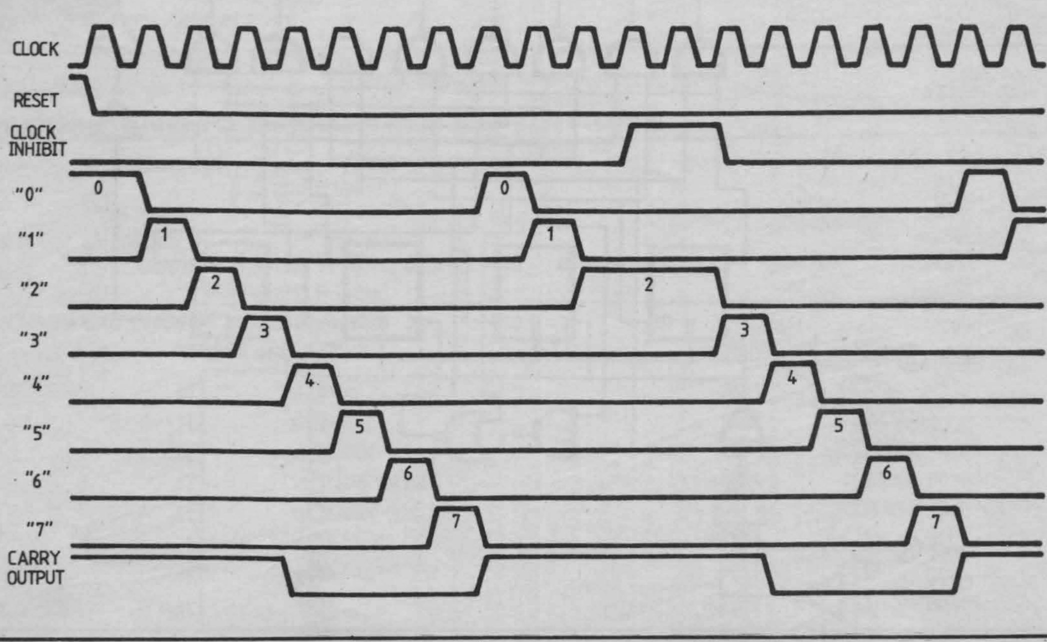


TIMING DIAGRAM

MMC 4017



MMC 4022



STATIC ELECTRICAL CHARACTERISTICS
(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T_{LOW}* min.	T_{LOW}* max.	25°C min.	25°C typ	25°C max.	T_{HIGH}* min.	T_{HIGH}* max.	
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall times = 20 ns)

PARAMETER		TEST CONDITIONS V_{DD}(V)	VALUES min.	typ.	max.	UNIT
Clocked operation						
t_{PLH}, t_{PHL}	Propagation delay time Decode out	5 10 15		325 135 85	650 270 170	ns
	Carry out	5 10 15		300 125 80	600 250 160	ns
t_{THL}, t_{TLH}	Transition time Carry Out or Decoded Out Line	5 10 15		80 100 50	200 100 80	ns
f_{CL}	Minimum clock input frequency	5 10 15	2.5 5 5.5	5 10 11	5	MHz
t_w	Maximum clock pulse width	5 10 15		100 45 30	200 90 60	ns
t_r t_f	Clock input rise or fall time	5 10 15	Unlimited			µs
t_{setup}	Data setup time Minimum clock inhibit	5 10 15		115 50 35	230 100 75	ns

Reset operation

PARAMETER		TEST CONDITIONS V_{DD}(V)	min.	typ.	max.	UNIT
t_{PLH}, t_{PHL}	Propagation delay time Carry Out or Decoded Out Line	5 10 15		265 115 85	530 230 170	ns
t_W	Minimum reset pulse width	5 10 15		130 55 30	260 110 60	ns
t_{rem}	Minimum reset removal time	5 10 15		200 140 75	400 280 150	ns

PRESSETTABLE DIVIDE-BY-N COUNTER

GENERAL DESCRIPTION

The MMC 4018 (G and H types) and MMC 4018 (E and F types) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package, ceramic flat package and plastic micropackage.
The MMC 4018 types consists of 5 Johnson-Counter stages, buffered $\overline{Q}$ outputs from each stage, and counter preset control gating. CLOCK, RESET, DATA, PRESET ENABLE, and 5 individual JAM inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the $\overline{Q5}$, $\overline{Q4}$, $\overline{Q3}$, $\overline{Q2}$, $\overline{Q1}$ signals, respectively, back to the DATA input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of a MMC 4011 gate package to properly gate the feedback connection to the DATA input. Divide-by-functions greater than 10 can be achieved by use of multiple MMC 4018 units. The counter is advanced one count at the positive clock-signal transition. Schmitt-Trigger action on the clock line permits unlimited clock rise and fall times. A high RESET signal clears the counter to an all-zero condition. A high PRESET-ENABLE signal allows information on the JAM inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

FEATURES

- Medium speed operation 10 MHz (typ.) at $V_{DD}-V_{SS} = 10$ V.
- Fully static operation.

ABSOLUTE MAXIMUM RATINGS

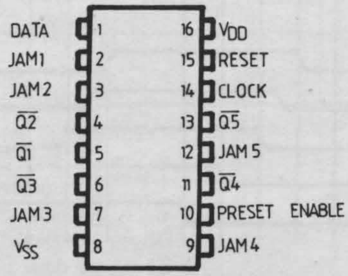
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

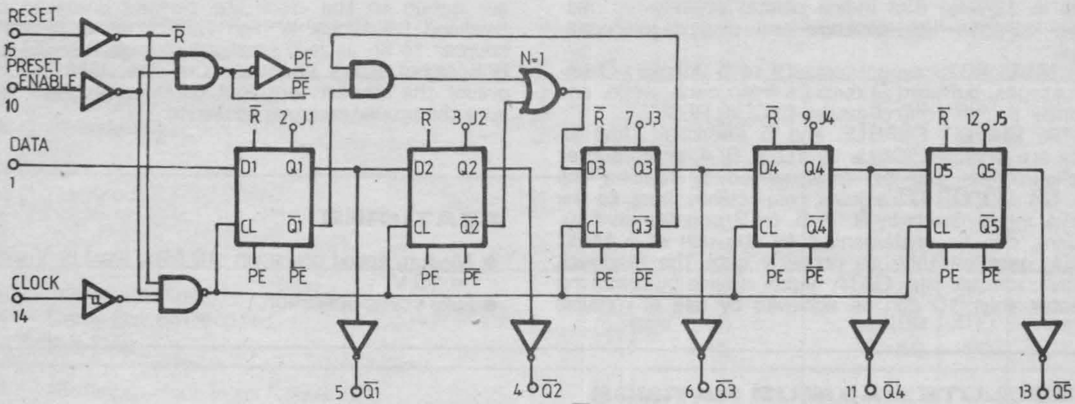
RECOMMENDED OPERATING CONDITIONS

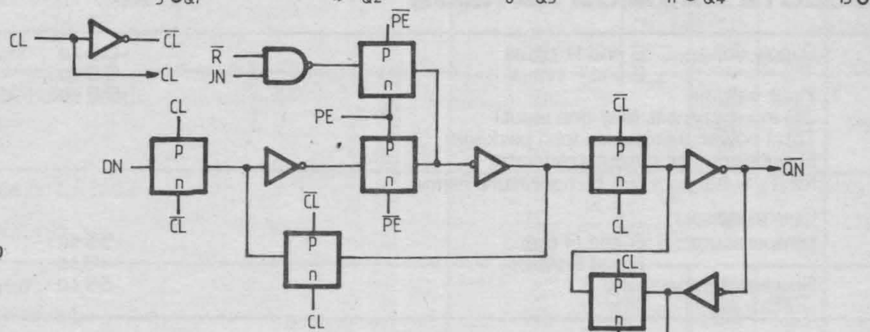
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	In put voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



LOGIC DIAGRAM

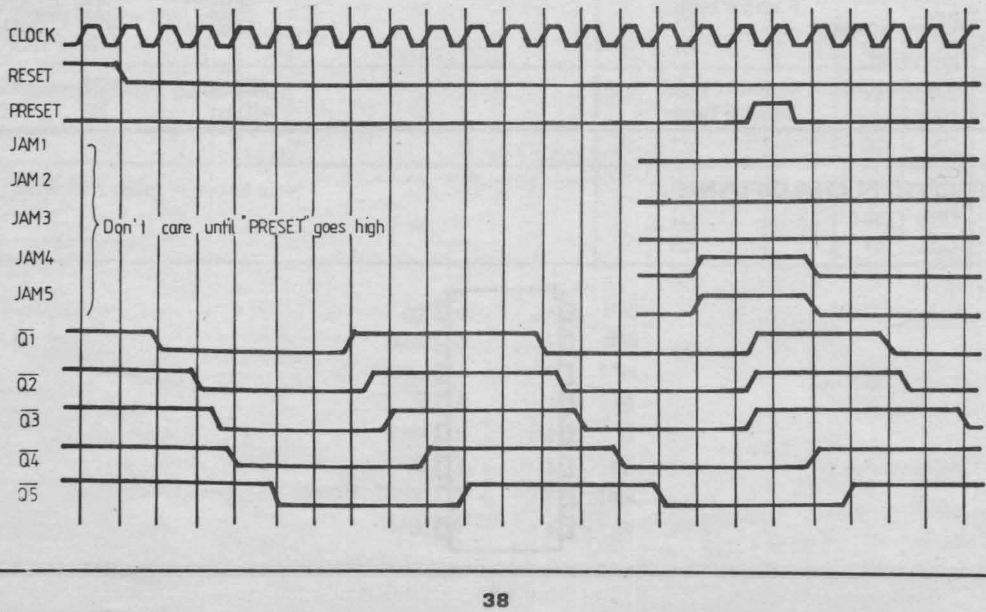




Detail for flip-flop

TIMING DIAGRAM

(Data input tied to $\overline{Q5}$ for decade counter configuration)



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} =$ 5 V

2 V min. with $V_{DD} =$ 10 V

2.5 V min. with $V_{DD} =$ 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns).

	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES			UNIT
			min.	typ.	max.	
t_{PLH}, t_{PHL}	Propagation delay time	5 10 15		200 90 65	400 180 130	ns
t_{THL}, t_{TLH}	Transition time	5 10 15		100 50 40	200 100 80	ns
f_{CL}	Maximum clock input frequency	5 10 15	3 7 8.5	6 14 17		MHz
t_W,	Clock pulse width	5 10 15	160 70 50	80 35 25		ns
t_r, t_f	Clock input rise or fall time	5 10 15	Unlimited			μs
t_{setup}	Data input Set-Up time	5 10 15	40 12 6	20 6 3		ns
t_H	Data input Hold-time	5 10 15	140 80 60	70 40 30		ns
Preset* or reset operation						
t_{PLH}, t_{PHL}	Propagation delay time (Reset or Reset to $\overline{Q}$)	5 10 15		275 125 90	550 250 180	ns
t_w	Preset or reset pulse width	5 10 15	160 70 50	80 35 25		ns
t_{rem}	Preset or reset removal time	5 10 15	80 30 20	40 15 10		ns

* At PRESET ENABLE OR JAM inputs.

QUAD AND/OR SELECT GATE

GENERAL DESCRIPTION

The MMC 4019 consists of four AND/OR select gate configurations, each consisting of two input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_a and K_b. In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical A + B function.
The MMC 4019 E/F/G/H types are supplied in 16-lead hermetic dual-in-line ceramic or plastic package.

FEATURES

- Medium-speed operation $t_{PHL} = t_{PLH} = 60$ ns (TYP.) at $V_{DD} = 10$ V, $C_L = 50$ pF
- 100% tested for quiescent current

APPLICATIONS

- AND-OR select gating
- Shift-right/shift/left registers
- True/complement selection
- And-OR/exclusive-OR selector

ABSOLUTE MAXIMUM RATINGS

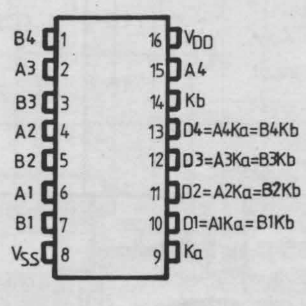
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			± 10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	In put voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
							min.	max.	min.	typ	max.	min.	max.	
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.
The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kΩ, typical temperahure coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

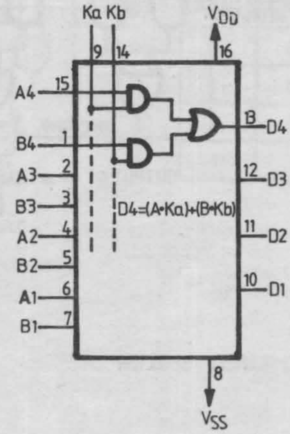
PARAMETER		TEST CONDITIONS		VALUES		UNIT
		V_{DD}(V)	min.	typ.	max.	
t_{PLH}, t_{PHL}	Propagation delay time	5 10 15		150 60 50	300 120 100	ns
t_{TLH}, t_{TLH}	Transition time	5 10 15		100 50 40	200 100 80	ns

TRUTH TABLE

K_a	K_b	A_n	B_n	DN
1	0	1	X	1
1	0	0	X	0
0	1	X	1	1
0	1	X	0	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

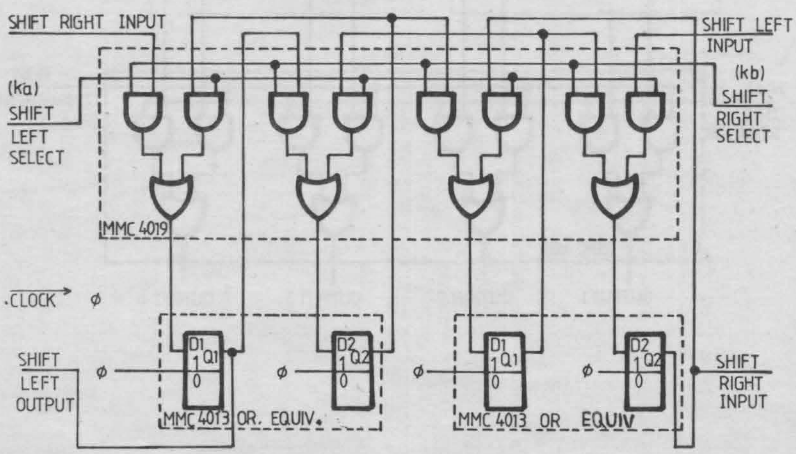
X = Don't Care

LOGIC DIAGRAM

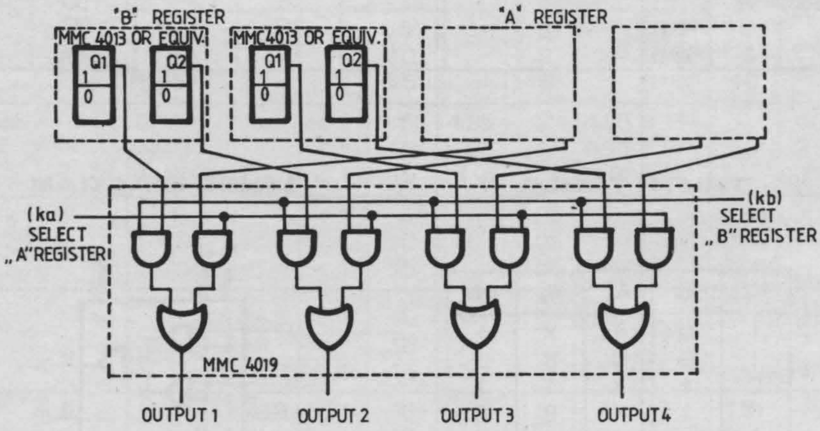


TYPICAL APPLICATIONS

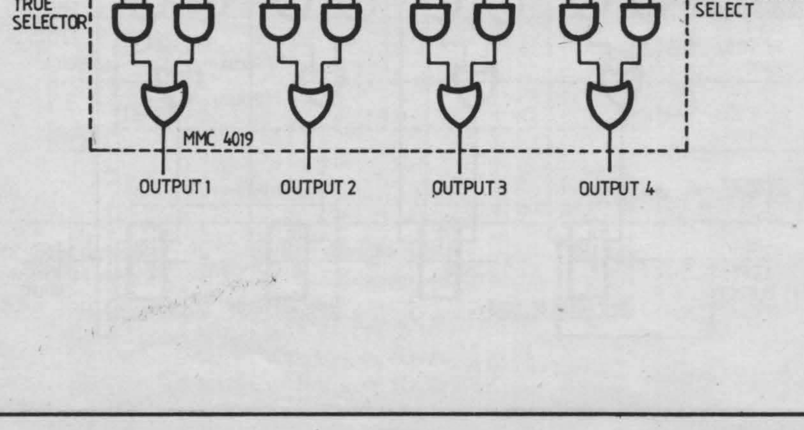
SHIFT-LEFT SHIFT-RIGHT REGISTER



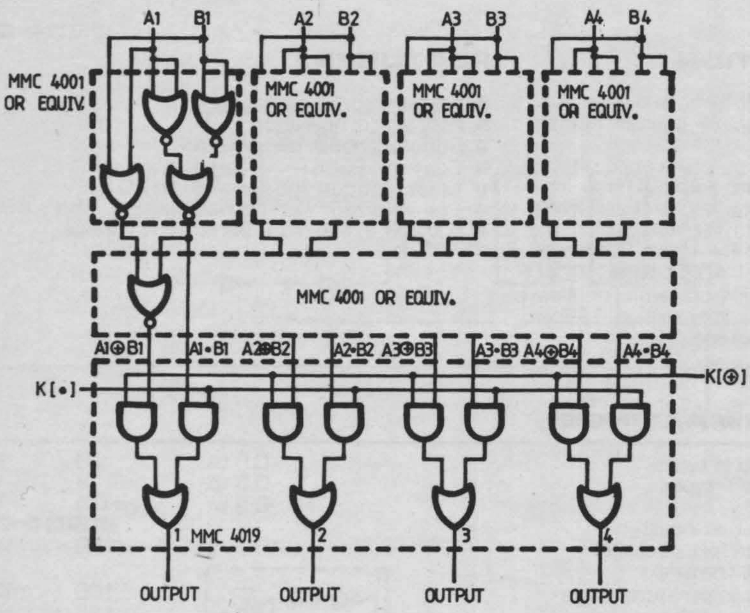
AND-OR SELECTED GATING



TRUE COMPLEMENT SELECTOR



AND-OR exclusive OR selector



TRUTH TABLE

K[•]	K[⊕]	OUT
0	0	0
1	0	A • B
0	1	A ⊕ B
1	1	A + B

RIPPLE-CARRY BINARY COUNTER/DIVIDERS:

4020 - 14 STAGE
4024 - 7 STAGE
4040 - 12 STAGE

GENERAL DESCRIPTION

These devices are monolithic I.C's fabricated with standard AL-gate CMOS technology. All counter stages are master-slave flip-flops.
The state of a counter advances one count on the negative transition of each input pulse. A high level on the RESET line resets the counter to its all zeros stage. Schmitt trigger action on the input-pulse line permits unlimited clock rise and fall times. All inputs and outputs are buffered. MMC 4020, MMC 4040 are available in 16-lead dual-in-line ceramic or plastic package and MMC 4024 is available in 14-lead dual-in-line plastic or ceramic package.

FEATURES

- Medium-speed operation
- Fully static operation
- Buffered inputs and outputs
- Common RESET
- Quiescent current specified to 20 V
- Standardized symmetrical output characteristics
- 5 V, 10 V, and 15 V parametric ratings

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_i	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		±10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

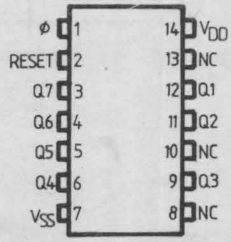
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_i	In put voltage	0 to	V_{DD}	V
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

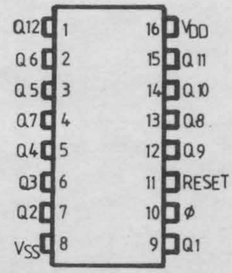
CONNECTION DIAGRAM

MMC 4020

MMC 4024

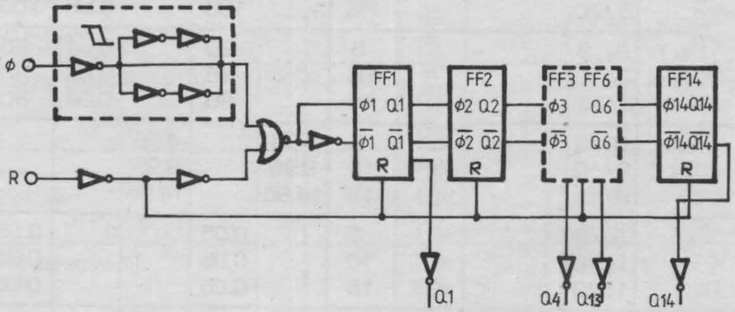


MMC 4040

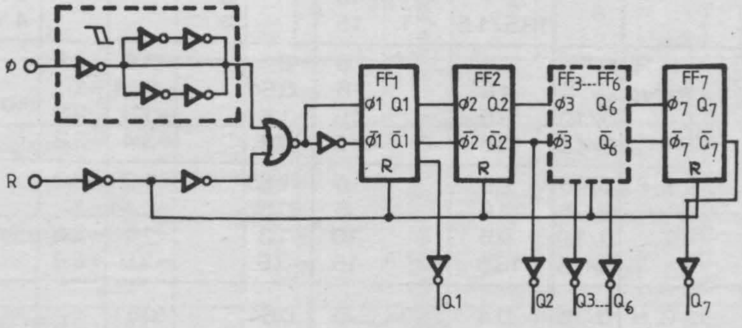


LOGIC DIAGRAM

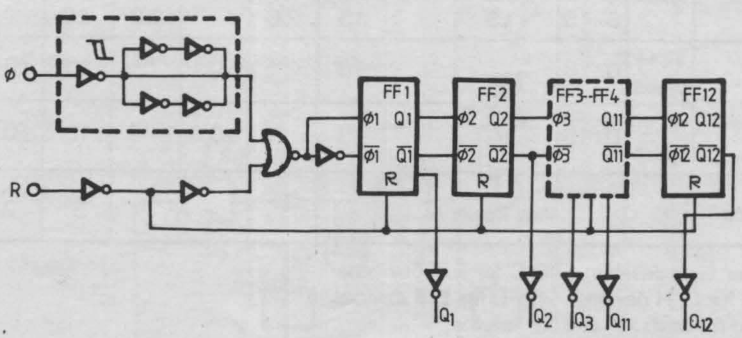
MMC 4020



MMC 4024



MMC 4040



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15	Any input		15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

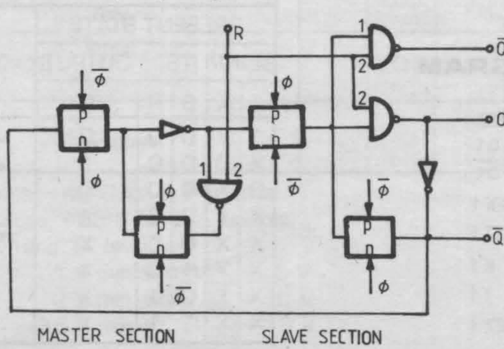
1 V min. with $V_{DD} =$ 5 V
2 V min. with $V_{DD} =$ 10 V
2.5 V min. with $V_{DD} =$ 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A \doteq 25°C$, $C_L = 50$ pF, $R_L = 200$ kohm, typical temperature coefficient for all $V_{DD} = 0.3\%/°C$ values, all input rise and fall time = 20 ns)

	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES min.	VALUES typ.	VALUES max.	UNIT
Input pulse operation						
t_{PLH}, t_{PHL}	Propagation delay time (Φ to Q1 Out)	5 10 15		180 80 65	360 160 130	ns
t_{PLH}, t_{PHL}	Propagation delay time Qn to Qn+1	5 10 15		100 40 30	200 80 60	ns
t_{TLH}, t_{THL}	Transition time	5 10 15		100 50 40	200 100 80	ns
t_W	Minimum input pulse width	5 10 15		70 30 20	140 60 40	ns
t_r, t_f	Input rise and fall time	5 10 15		Unlimited		μs
f_{max}	Maximum input clock frequency	5 10 15	3.5 8 12	7 16 24		MHz
Reset operation						
t_{PHL}	Propagation delay time	5 10 15		140 60 50	280 120 100	ns
t_W	Minimum reset pulse width	5 10 15		100 40 30	200 80 60	ns
t_{rem}	Reset removal time	5 10 15		175 75 50	350 150 100	ns

Detail of flip-flop stage



DUAL J-K MASTER SLAVE FLIP-FLOP

GENERAL DESCRIPTION

The MMC 4027 is a monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package.

The MMC 4027 is a single monolithic chip integrated circuit containing two identical complementary-simmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K, Set, Reset and Clock input signals. Buffered Q and $\overline{Q}$ signals are provided as outputs. This input-output arrangement provides for compatible operation with the MMC 4013 dual D-type flip-flop.
The MMC 4027 is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.

FEATURES

- Set-Reset capability
- Static flip-flop operation-retains state indefinitely with clock level either „high" or „low"
- Medium speed operation-16 MHz (typ.) clock toggle rate at 10 V
- 100% tested for quiescent current

APPLICATIONS

- Registers, counters, control circuits

ABSOLUTE MAXIMUM RATINGS

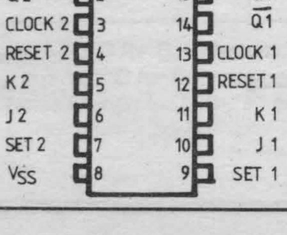
V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_i	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		± 10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature: G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_i	Imput voltage	0 to	V_{DD}	V
T_A	Operating temperature: G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



PRESENT STATE					CL•	NEXT STATE OUTPUTS		
INPUTS				OUTPUT				
J	K	S	R	Q		Q	$\overline{Q}$	
1	X	0	0	0	↑	1	0	
X	0	0	0	1	↑	1	0	
0	X	0	0	0	↑	0	1	
X	1	0	0	1	↑	0	1	
X	X	0	0	X	↓			←NO CHANGE
X	X	1	0	X	X	1	0	
X	X	0	1	X	X	0	1	
X	X	1	1	X	X	1	1	

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

Parameter			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	Unit
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

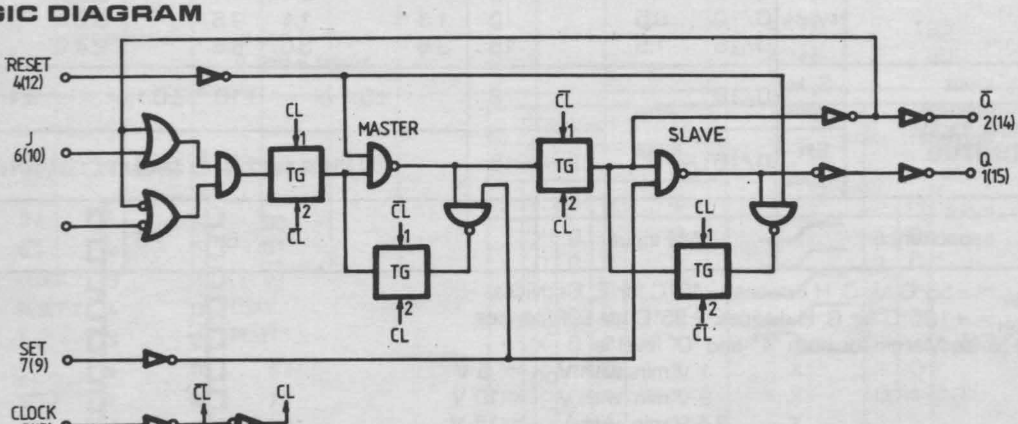
DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

	PARAMETER		TEST CONDITIONS V_{DD}(V)	VALUES Min.	Typ.	Max.	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	Clock to or Q outputs	5		150	300	
			10		65	130	ns
			15		45	190	
t_{PLH}	Propagation delay time	Set to Q or Reset to $\overline{Q}$	5		150	300	
			10		65	130	
			15		45	90	
t_{PHL}	Propagation delay time	Set to $\overline{Q}$ or Reset to Q	5		200	400	ns
			10		85	170	
			15		60	120	
t_{THL}, t_{TLH}	Transition time		5		100	200	
			10		50	100	ns
			15		40	80	
t_W	Pulse width	Clock	5	140	70		
			10	60	30		
			15	40	20		
t_W	Pulse width	Set or Reset	5	180	90		ns
			10	80	40		
			15	50	25		
t_r, t_f	Clock input rise or fall time		5			15	
			10			4	ns
			15			1	
t_{setup}	Setup time	Data	5	200	100		
			10	75	35		ns
			15	50	25		
f_{max}	Maximum clock input frequency*	Toggle mode	5	3.5	7		
			10	8	16		MHz
			15	12	24		

* Input t_r, $t_f = 5$ ns.

LOGIC DIAGRAM



BCD-TO-DECIMAL DECODER

GENERAL DESCRIPTION

The MMC 4028 is a BCD-to-decimal or binary-to-octal decoder. This device is a monolithic IC fabricated in standard Al-gate CMOS technology. MMC 4028 is available in 16-lead dual in line ceramic and plastic package. The MMC 4028 consists of buffering on all four inputs decoding-logic gates, and 10 output buffers. A BCD code applied to the four inputs. A to D, results in a high level at the selected one of ten decimal decoded outputs. High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

FEATURES

- High decoded output drive capability
- Medium speed operation
- „Positive logic" inputs and outputs (decoded outputs go high on selection)

ABSOLUTE MAXIMUM RATINGS

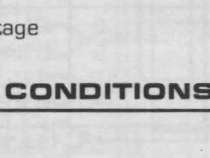
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			± 10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Imput voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15	Any input		15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

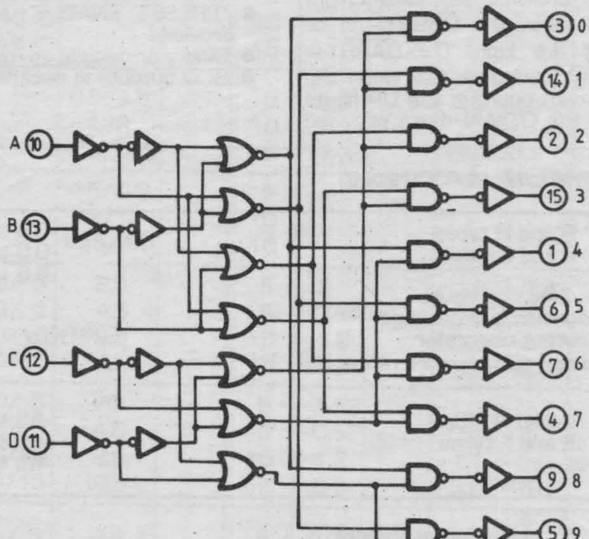
* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 K, typical temperature coefficient for all V_{DD} values is 0.3 %/°C all input rise and fall times= 20 ns)

	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES min.	VALUES typ.	VALUES max.	UM
t_{PHL}, t_{PLH}	Propagation delay time (clock to out)	5		175	350	ns
		10		80	160	
		15		60	120	
t_{THL}, t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	

LOGIC DIAGRAM



TRUTH TABLE

D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

WHERE 1 = HIGH LEVEL
0 = LOW LEVEL

PRESETTABLE UP/DOWN COUNTER BINARY OR BCD-DECADE

GENERAL DESCRIPTION

The MMC 4029 is a monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package.
The MMC 4029 consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single CLOCK, $\overline{\text{CARRY—IN}}$ ($\overline{\text{CLOCK ENABLE}}$), BINARY/DECADE, UP/DOWN, PRESET ENABLE signals. Q1, Q2, Q3, Q4 and a $\overline{\text{CARRY OUT}}$ signal are provided as outputs. A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock. A low on each JAM line, when the PRESET—ENABLE signal is high, resets the counter to it's zero count. The counter is advanced one count at the positive transition of the clock when the $\overline{\text{CARRY—IN}}$ or PRESET ENABLE signals are high. Advancement is inhibited when the $\overline{\text{CARRY—IN}}$ or PRESET ENABLE signals are high. The $\overline{\text{CARRY—OUT}}$ signal is normally high and goes low when the counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided the $\overline{\text{CARRY—IN}}$ signal is low. The $\overline{\text{CARRY—IN}}$ signal in the low state can thus be considered a $\overline{\text{CLOCK ENABLE}}$. The $\overline{\text{CARRY—IN}}$ terminal must be conected to V_{SS} when not in use. Binarv counting is accomplished when the BINARY/DECADE input is high; the counter counts in the decade mode when the BINARY/DECADE input is low.
Multiple packages can be conected in either a parallel-clocking or a ripple-clocking arrangement as shown in cascading counter packages. Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

FEATURES

- Medium speed operation—8 MHz (typ.) at C_L = 50 pF and $V_{DD}—V_{SS}$ = 10 V
- Multi-package parallel clocking for synchronous high speed output response or ripple clocking for slow clock input rise and fall times
- "PRESET ENABLE" and individual "JAM" inputs provided
- Binary or decade up/down counting
- BCD outputs in decade mode

ABSOLUTE MAXIMUM RATINGS

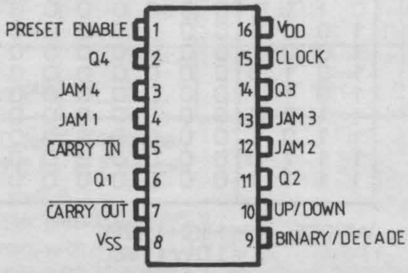
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Imput voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.
The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kΩ, typical temperature coefficient for all $V_{DD} = 0.3\%/°C$, all input rise and fall times ≤ 20 ns)

	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES min.	VALUES typ.	VALUES max.	UNIT
Clocked operation						
t_{PLH}, t_{PHL}	Propagation delay time (Q outputs)	5		250	500	ns
		10		120	240	
		15		90	180	
t_{PLH}, t_{THL}	Propagation delay time (Carry Output)	5		280	560	
		10		130	260	
		15		95	190	
t_{TLH}, t_{THL}	Transition time (Q outputs, carry output)	5		100	200	ns
		10		50	100	
		15		40	80	
t_W,	Minimum clock pulse width	5		90	180	ns
		10		45	90	
		15		30	60	
t_r, t_f*	Clock rise and fall time	5			15	µs
		10			15	
		15			15	
t_{setup}**	Minimum setup time (Carry input)	5		30	60	ns
		10		10	20	
		15		6	12	
t_{setup}	Minimum setup time (B/D or U/D)	5		170	340	
		10		70	140	
		15		50	100	
f_{max}	Maximum clock input frequency	5	2	4		MHz
		10	2	8		
		15	5.5	11		
Preset enable						
t_{THL}, t_{TLH}	Propagation delay time (Q outputs)	5		235	470	ns
		10		100	200	
		15		80	160	
t_{PHL}, t_{PLH}	Propagation delay time (Carry Output)	5		320	640	
		10		145	290	
		15		105	210	
t_W,	Minimum Preset enable (pulse width)	5		65	130	ns
		10		35	70	
		15		25	50	
t_{rem}**	Minimum preset enable (removal time)	5		100	200	ns
		10		55	110	
		15		40	80	
Carry input						
t_{PHL}, t_{PLH}	Propagation delay time (Carry output)	5		170	340	ns
		10		70	140	
		15		50	100	
t_{setup}***	Minimum setup time (Carry input)	5		25	50	ns
		10		15	30	
		15		12	25	

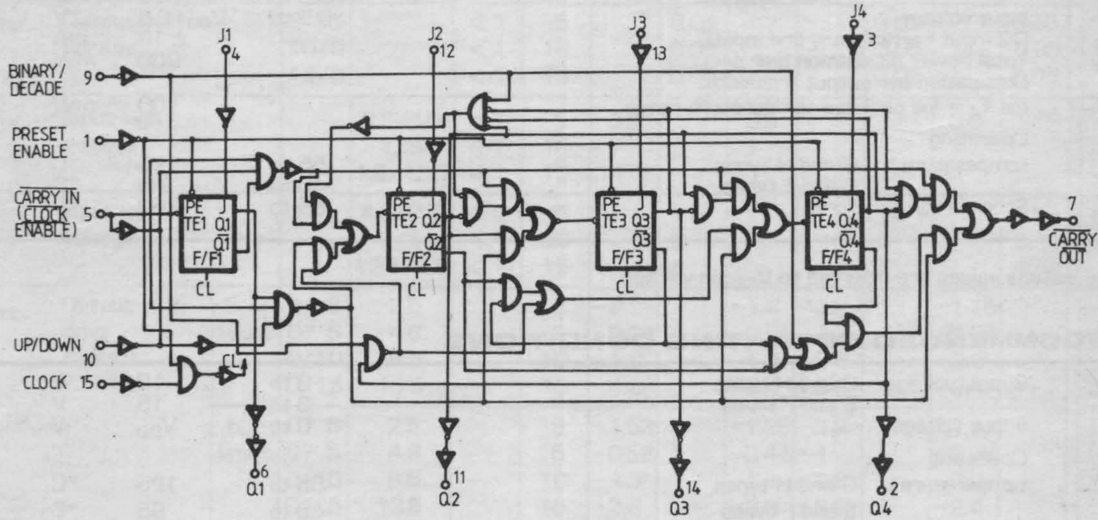
PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES min.	VALUES typ.	VALUES max.	UNIT
t_{hold}*** Minimum hold time (Carry input)	5 10 15		100 35 30	200 70 60	ns

* If more than one unit is cascaded in the parallel clocked application, t_r should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.

** From Up/Down, Binary/Decade, Carry In preset Enable Control Inputs to Clock Edge.

*** From Carry In to Clock Edge.

LOGIC DIAGRAM



TRUTH TABLES

CLOCK	TE	PE	J	Q	$\overline{Q}$
X	X	0	0	0	1
⌐_ (falling)	0	1	X	$\overline{Q}$	Q
X	X	0	1	1	0
⌐_ (falling)	1	1	X	Q	$\overline{Q}$ NC
_⌐ (rising)	X	1	X	Q	$\overline{Q}$ NC

X = don't care

CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC (B/D)	1 0	BINARY COUNT DECADE COUNT
UP/DOWN (U/D)	1 0	UP COUNT DOWN COUNT
PRESET ENABLE (PE)	1 0	JAM IN NO JAM
$\overline{\text{CARRY IN}}$ ($\overline{\text{CI}}$) (CLOCK ENABLE)	1 0	NO COUNTER ADVANCE AT POSITIVE CLOCK TRANSITION COUNTER ADVANCE AT POSITIVE CLOCK TRANSITION

QUAD EXCLUSIVE-OR GATE

GENERAL DESCRIPTION

The MMC 4030 is a monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package.
The MMC 4030 consists of four independent Exclusive-OR gates integrated on a single monolithic silicon chip. All inputs and outputs are protected against electrostatic effects.

FEATURES

- MEDIUM-SPEED OPERATION-$t_{PHL} = t_{PLH} = 65$ ns (TYP.) AT $C_L = 50$ pF and $V_{DD}-V_{SS} = 10$ V
- LOW OUTPUT IMPEDANCE: 500 Ω (TYP.) AT $V_{DD}-V_{SS} = 10$ V

APPLICATIONS

- Even and odd-parity generators and checkers
- Logical comparators
- Adders/substractors
- General logic functions

ABSOLUTE MAXIMUM RATINGS

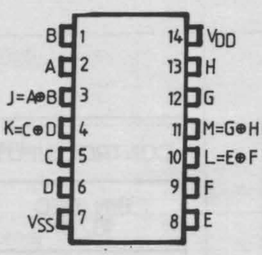
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

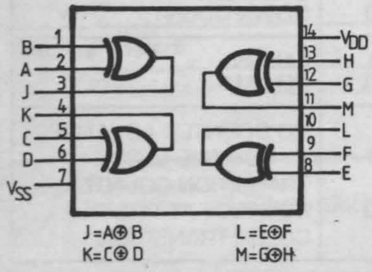
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Imput voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM



TRUTH TABLE

One of four identical gates

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

Where „1" = High level
„0" = Low level

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

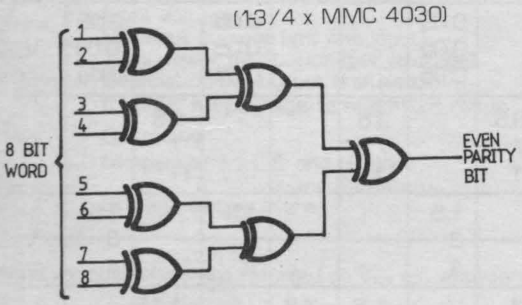
DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20 ns).

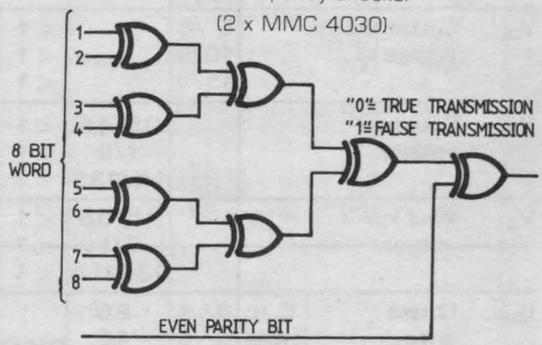
PARAMETER		TEST CONDITIONS	VALUES			UNIT
		V_{DD} (V)	min	typ	max	
t_{PLH}, t_{PHL}	Propagation delay time	5 10 15		140 65 50	280 130 100	ns
t_{TLH} t_{THL}	Transition time	5 10 15		100 50 40	200 100 80	ns

TYPICAL APPLICATIONS

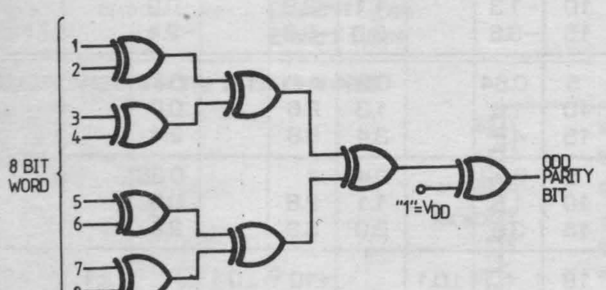
Even-parity-bit generator
(1-3/4 x MMC 4030)



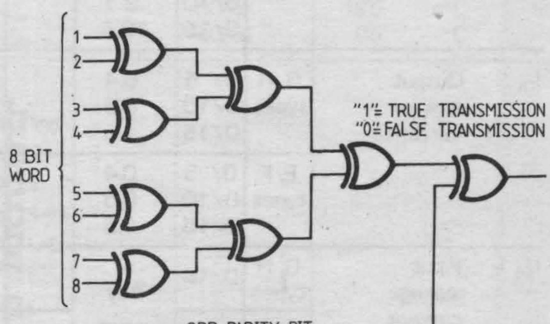
Even-parity checker
(2 x MMC 4030)



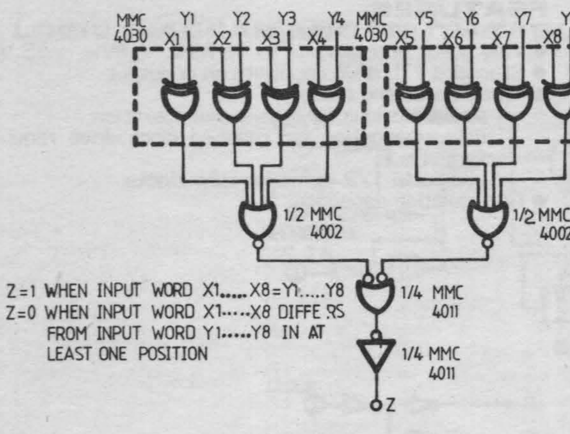
Odd-parity-bit generator
(2 x MMC 4030)



Odd-parity checker
(2 x MMC 4030)



8-bit comparator



8-bit two's complement adder-substractor

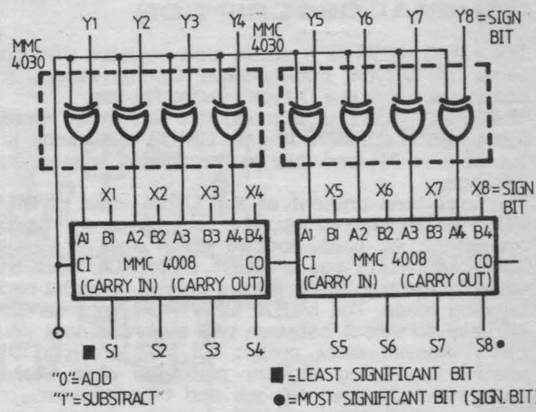


TABLE 1

Two's complement numbers and their equivalent decimal values

X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1
0	0	0	0	0	0	0	0 = 0	1	1	1	1	1	1	1	1 = − 1
0	0	0	0	0	0	0	1 = 1	1	1	1	1	1	1	1	0 = − 2
0	0	0	0	0	0	1	0 = 2	1	1	1	1	1	1	0	1 = − 3
0	0	0	0	0	0	1	1 = 3	1	1	1	1	1	0	1	1 = − 4
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
0	1	1	1	1	1	1	0 = 126	1	0	0	0	0	0	0	1 = −127
0	1	1	1	1	1	1	1 = 127	1	0	0	0	0	0	0	0 = −128

The two's complement adder-substractor can add or substract any two of the numbers in TABLE 1.

For example

a)

	SIGN BIT								
2 + −5 = X	0	0	0	0	0	0	1	0	2 +
−Y	1	1	1	1	1	0	1	1	−5 +
CI								0	
S 0 (CO)	1	1	1	1	1	1	0	1	= −3

b)

	SIGN BIT								
−2 − −5 = X	1	1	1	1	1	1	1	0	−2 +
Y	1	1	1	1	1	0	1	1	−5
$\overline{Y}$	0	0	0	0	0	1	0	0	+
CI									
S 1 (CO)	0	0	0	0	0	0	1	1	= 3

64-STAGE STATIC SHIFT REGISTER

GENERAL DESCRIPTION

The MMC 4031 is a static shift register that contains 64 D-type, master-slave flip-flop stages and one stage which is a D-type master flip-flop.
The MMC 4031 is a monolithic integrated circuit, fabricated in standard Al-gate CMOS technology. It is available in 16-lead dual in-line plastic and ceramic package.
The logic level present at the DATA input of MMC 4031 is transferred into the first stage and shifted one stage at each positive-going clock transition. The MMC 4031 has a MODE CONTROL input that when in the high state, allows operation in the recirculating mode. The MODE CONTROL input can also be used to select between two separate data sources. A delayed clock output (CL_D) is provided that enables cascading register packages while allowing reduced clock drive fan-out and transition-time requirements. A third cascading option makes use of the Q' output from the 1/2 stage, which is available on the next negative-going transition of the clock after the Q output occurs. This delayed output is used with clocks having slow rise and fall times.

FEATURES

- Fully static operation: dc to 16 MHz, $V_{DD}-V_{SS} = 15$ V
- Standard TTL drive capability on Q output
- Three cascading modes:
  - -- direct clocking for high-speed operation
  - -- delayed clocking for reduced clock drive requirements
  - -- additional 1/2 stage for slow clocks
- Recirculation capability

ABSOLUTE MAXIMUM RATINGS

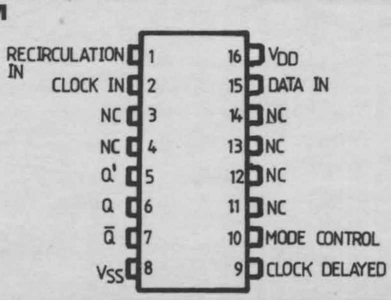
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	$V_{DD}+0.5$	V
I_I	DC input current (any one input)			± 10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

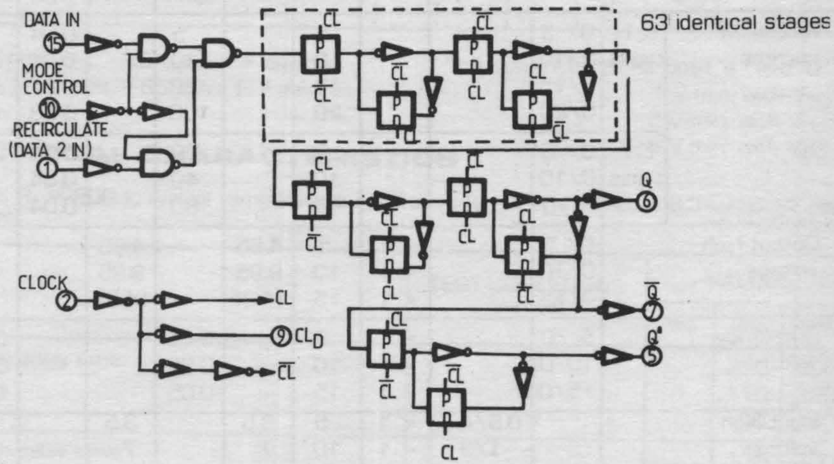
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



LOGIC DIAGRAM AND TRUTH TABLES



INPUT CONTROL CIRCUIT

DATA	RECIRC.	MODE	BIT INTO STAGE 1
1	X	0	1
0	X	0	0
X	1	1	1
X	0	1	0

1 = HIGH LEVEL, 0 = LOW LEVEL,
X = DON'T CARE

OUTPUT FROM Q' (PIN 5)

Data + 64	CL	Data + 64.5
0		0
1		1
X		NC

1 = HIGH LEVEL, 0 = LOW LEVEL,
X = DON'T CARE, NC = NO CHANGE

TYPICAL STAGE

Data	CL	Data + 1
0		0
1		1
X		NC

1 = HIGH LEVEL, 0 = LOW LEVEL,
X = DON'T CARE, NC = NO CHANGE

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output source current (source) Q, $\overline{Q}$, Q CL_D	G, H types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		E, F types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I_{OL}	Output sink current Q	G, H types	0/ 5	0.4		5	2.56		2.04	4		1.44		mA
			0/10	0.5		10	6.4		5.2	10.4		3.6		
			0/15	1.5		15	16.8		13.6	27.2		9.6		
		E, F types	0/ 5	0.4		5	2.08		1.74	4		1.43		
			0/10	0.5		10	5.01		4.42	10.4		3.74		
			0/15	1.5		15	13.6		11.56	27.2		9.52		
I_{OL}	Output sink current $\overline{Q}$, Q' CL_D	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	

PARAMETER		TEST CONDITIONS				VALUES							UNIT
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
						min.	max.	min.	typ	max.	min.	max.	
C_I	Input capacitance	Any input							5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:
1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ k, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times= 20 ns)

PARAMETER		TEST CONDITIONS V_{DD} (V)	VALUES min.	typ.	max.	UNIT
t_{PHL}, t_{PLH} t_{PLH}	Propagation delay time: Clock to $\overline{Q}$, Clock to Q	5 10 15		250 110 90	500 220 180	ns
t_{PHL}, t_{PLH} t_{PHL}	Propagation delay time: Clock to Q' Clock to Q	5 10 15		190 80 65	380 160 130	ns
	Clock to CL_D	5 10 15		100 50 40	200 100 80	ns
t_{THL}, t_{TLH}	Transition time (any output, except Q t_{THL})	5 10 15		100 50 40	200 100 80	ns
t_{THL}	Q	5 10 15		50 25 20	100 50 40	ns
t_{setup}	Data setup time	5 10 15		30 15 10	60 30 20	ns
t_{hold},	Data hold time	5 10 15		30 15 10	60 30 20	ns
t_W,	Clock pulse width	5 10 15		120 50 40	240 100 80	ns
t_{max}	Maximum clock input frequency**	5 10 15	2 5 6	4 10 12		MHz
t_r, t_f*	Clock input rise or fall time	5 10 15			1000 1000 200	μs

* If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 50 pF and the transition time of the output driving stage.

** Maximum clock frequency for cascaded units;

a) Using delayed clock feature in recirculation mode:

$$f_{max} = \frac{1}{(n-1)\ CL_D\text{prop. delay} + Q\text{ prop. delay} + \text{set-up time}}$$

where n=number of packages.

b) Not using delayed clock:

$$f_{max} = \frac{1}{\text{propagation delay} + \text{set-up time}}$$

4-STAGE PARALLEL IN/PARALLEL OUT SHIFT REGISTER

GENERAL DESCRIPTION

The MMC 4035 (G and H types) and MMC 4035 (E and F types) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package The MMC 4035 integrated circuit is a four-stage clocked signal serial register with provision for synchronous PARALLEL inputs to each stage and SERIAL inputs to the first stage via J$\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial D flip-flop configuration when the register is in the serial mode (PARALLEL/SERIAL control low). Parallel entry into each register stage is permitted when the PARALLEL/SERIAL control is high. In the parallel or serial mode information is transfered on positive clock transition. When the TRUE/COMPLEMENT control is high, the true contents of the register are available at the output terminals. When the TRUE/COMPLEMENT control is low, the outputs are the complements of the data in the register. The TRUE/COMPLEMENT control functions asynchronously with respect to the CLOCK signal. J$\overline{K}$ input logic is provided on the first stage SERIAL input to minimize logic requirements particulary in counting and sequence-generation applications. With J$\overline{K}$ inputs connected together, the first stage becomes a D flip-flop. An asynchronous common RESET is also provided.

FEATURES

- 4-stage clocked shift operation
- Synchronous parallel entry on all 4 stages
- J$\overline{K}$ inputs on first stage
- Asynchronous TRUE/COMPLEMENT control an all outputs
- Static flip-flop operation; master-slave configuration
- Buffered inputs and outputs
- High speed 12 MHz (typ.) at V_{DD} = 10 V.

ABSOLUTE MAXIMUM RATINGS

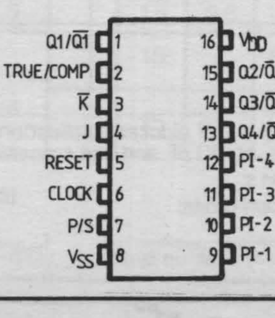
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

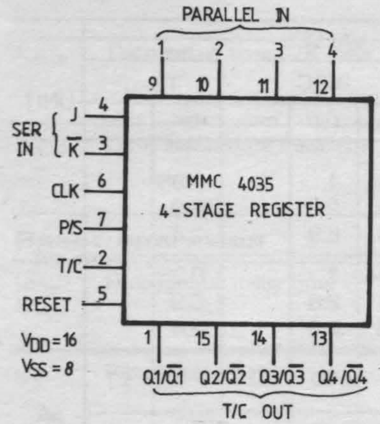
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM



TRUTH TABLE

FIRST STAGE

CLOCK	t_{n-1} (INPUTS)				t_n (OUTPUTS)
	J	K	R	Q_{n-1}	Q_n
$\uparrow$	0	X	0	0	0
$\uparrow$	1	X	0	0	1
$\uparrow$	X	0	0	1	0
$\uparrow$	1	0	0	Q_{n-1}	$\overline{Q}_{n-1}$ TOGGLE MODE
$\uparrow$	X	1	0	1	1
$\downarrow$	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

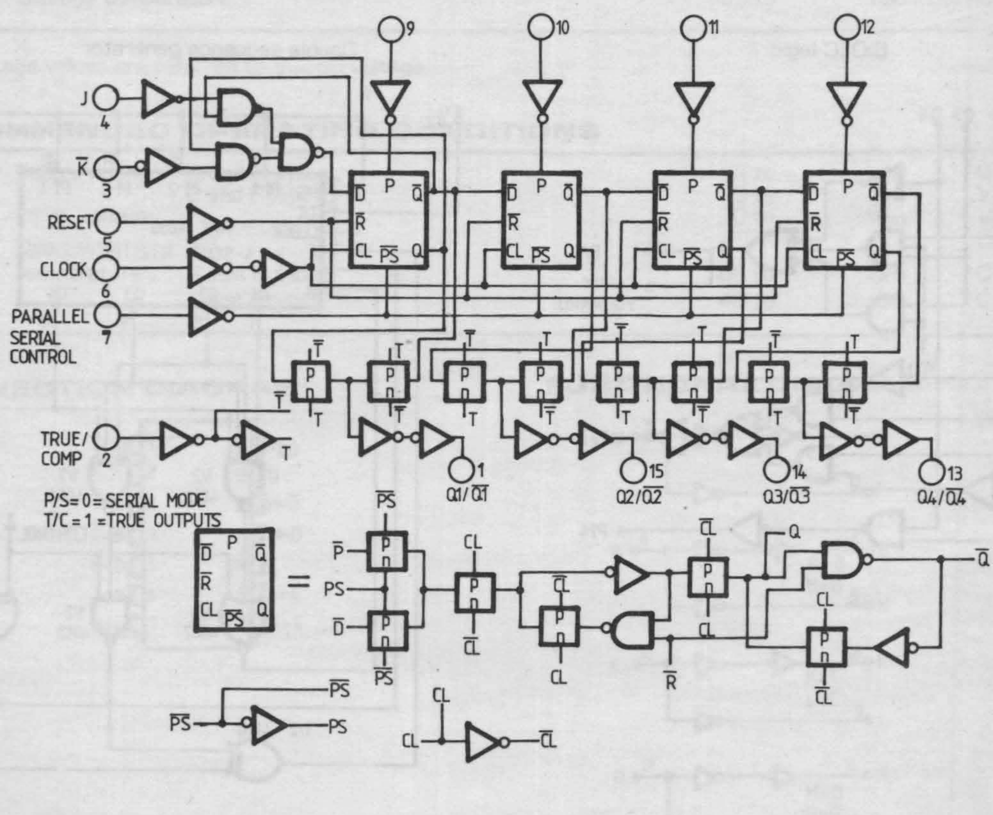
DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kohm, typical temperature coefficient for all $V_{DD} = 0.3\%/°C$ values, all input rise and fall time = 20 ns)

PARAMETER		TEST CONDITIONS V_{DD} (V)	VALUES min.	typ.	max.	Unit
Clocked operation						
t_{PLH}, t_{PHL}	Propagation delay time	5		250	500	ns
		10		100	200	
		15		75	150	
t_{THL}, t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
f_{CL}	Maximum clock input frequency	5	2	4		MHz
		10	6	12		
		15	8	16		
t_W	Clock pulse width	5		100	200	ns
		10		45	90	
		15		30	60	
t_r, t_f	Clock input rise or fall time	5		15		μs
		10		15		
		15		15		

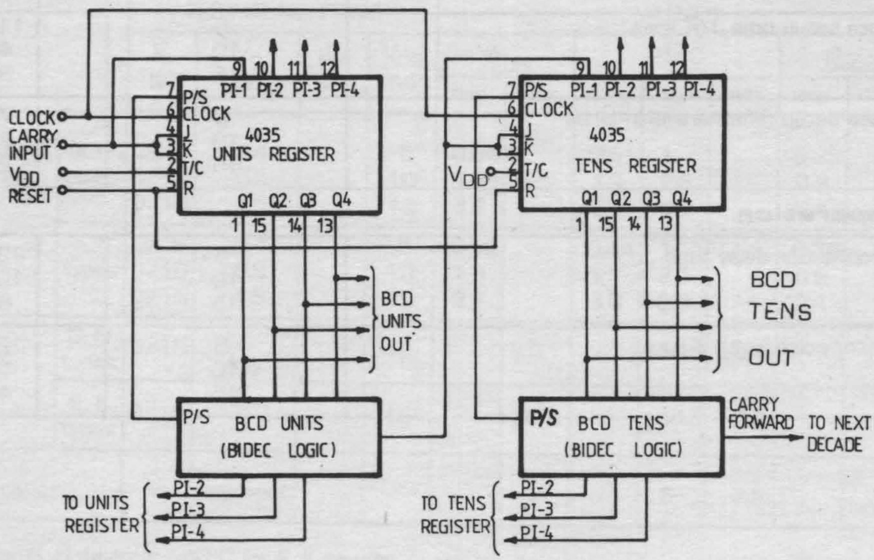
	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES			Unit
			min.	typ.	max.	
t_{setup}	Data setup time J/$\overline{K}$ lines	5 10 15		110 40 30	220 80 60	ns
t_{setup}	Data setup time Parallel-In-Lines	5 10 15		70 25 20	140 50 40	ns
Reset operation						
t_{PLH}, t_{PHL}	Propagation delay time	5 10 15		230 100 80	460 200 160	ns
t_W	Reset pulse width	5 10 15		125 55 40	250 110 40	ns

LOGIC DIAGRAM

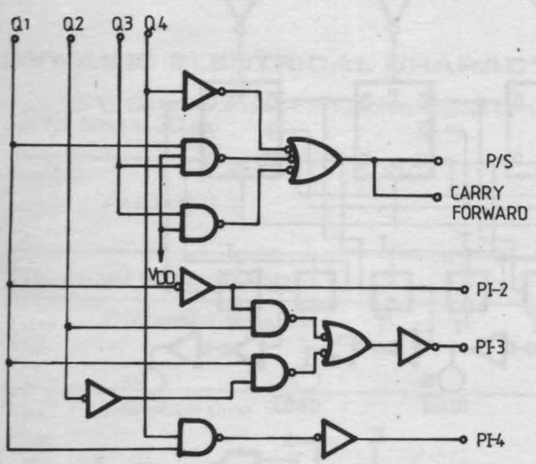


TYPICAL APPLICATIONS

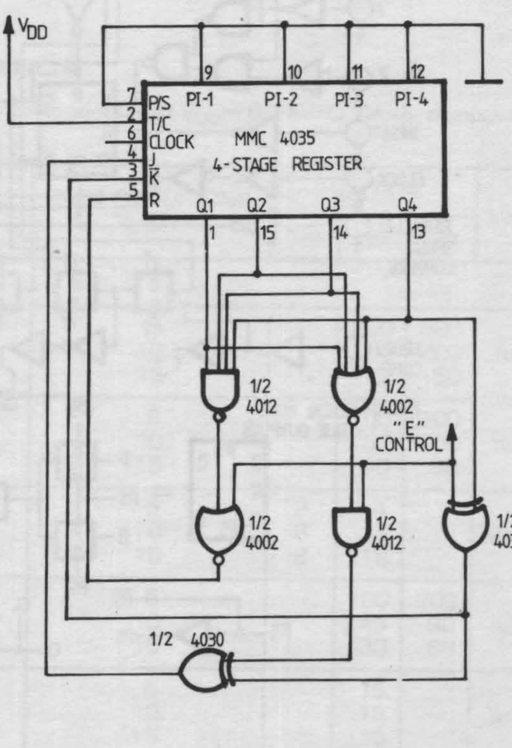
Binary — to — BCD converter



BIDEC logic



Double sequence generator



QUAD TRUE/COMPLEMENT BUFFER

GENERAL DESCRIPTION

The MMC 4041 is a monolitic integrated circuit processed in standard Al-gate CMOS technology. The MMC 4041 contains four true/complement buffers consisting of n- and p-channel units having low channel resistance and high current (sourcing and sinking) capability. The MMC 4041 is intended for use as a buffer, line driver, or CMOS-to-TTL driver. It can be used as an ultra-low power resistor-network driver for A/D and D/A conversion, as a transmission-line driver, and in other applications where high noise immunity and low-power dissipation are primary design requirements.

FEATURES

- Balanced sink and source current; approximately 4 times standard „B" drive
- Equalized delay to true and complement outputs

ABSOLUTE MAXIMUM RATINGS

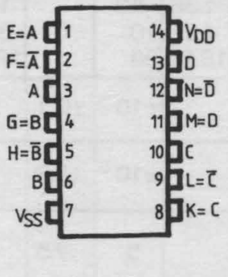
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	$V_{DD}+0.5$	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

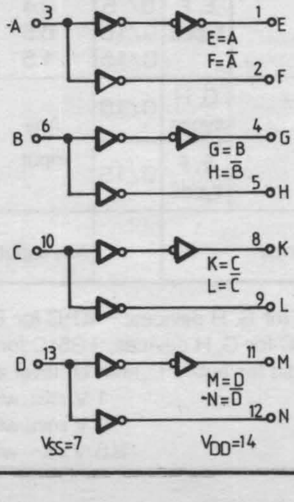
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	4		4			4		V
				1/9	< 1	10	8		8			8		
				1.5/13.5	< 1	15	12		12			13		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1			1.5		1.5	V
				9/1	< 1	10		2			3		3	
				13.5/1.5	< 1	15		2,5			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	-8.4		-6.4	-12.8		-4.6		mA
			0/ 5	4.6		5	-2.1		-1.6	-3.2		-1.2		
			0/10	9.5		10	-6.25		-5	-10		-3.5		
			0/15	13.5		15	-24		-19	-38		-13		
		E, F types	0/ 5	2.5		5	-6.8		-5.44	-12.8		-4.08		
			0/ 5	4.6		5	-1.7		-1.36	-3.2		-1.02		
			0/10	9.5		10	-5.31		-4.25	-10		-3.18		
			0/15	13.5		15	-20.18		-16.15	-38		-12.1		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	2.1		1.6	3.2		1.2		mA
			0/10	0.5		10	6.25		5	10		3.5		
			0/15	1.5		15	24		19	38		13		
		E, F types	0/ 5	0.4		5	1.7		1.36	3.2		1.02		
			0/10	0.5		10	5.31		4.25	10		3.18		
			0/15	1.5		15	20.18		16.15	38		12.11		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55$°C for G, H devices; -40°C for E, F devices.

* $T_{HIGH} = +125$°C for G, H devices; $+85$°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V

2 V min. with $V_{DD} = 10$ V

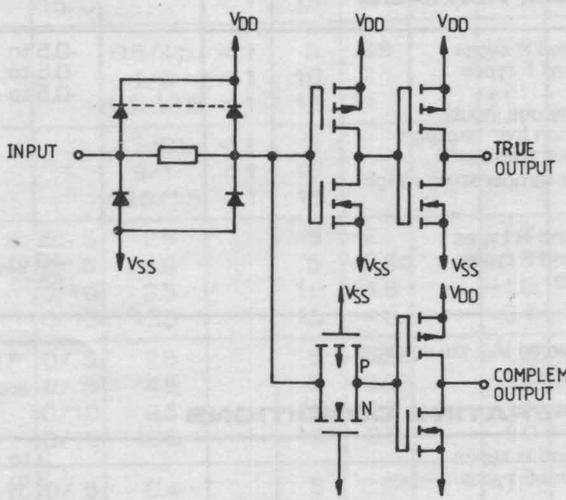
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

PARAMETER		TEST CONDITIONS	VALUES			UNIT
		VDD(V)	min.	typ.	max.	
t_{PLH}', t_{PHL}	Propagation delay time	5 10 15		60 35 25	120 70 50	ns
t_{THL} t_{THL}	Transition time	5 10 15		40 20 15	80 40 30	ns

SCHEMATIC DIAGRAM



QUAD CLOCKED „D" LATCH

GENERAL DESCRIPTION

The MMC 4042 is a monolithic integrated circuit, available in 16-lead dual in-line plastic package. The MMC 4042 contains four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit.
Information present at the data input is transferred to outputs Q and $\bar{Q}$ during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the I CLOCK level. The outputs follow the data input providing the CLOCK and POLARITY levels defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) the information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.

FEATURES

- Medium-speed operation
- Fully static operation
- Low power TTL compatible
- Common CLOCK
- Buffered inputs and outputs

ABSOLUTE MAXIMUM RATINGS

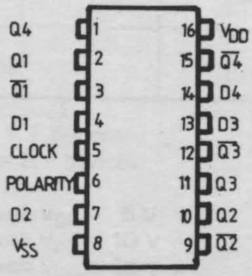
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T_{LOW}*		25°C			T_{HIGH}*		
							min.	max.	min.	typ	max.	min.	max.	
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		<1	5	4.95		4.95			4.95		V
			0/10		<1	10	9.95		9.95			9.95		
			0/15		<1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		<1	5		0.05			0.05		0.05	V
			10/0		<1	10		0.05			0.05		0.05	
			15/0		<1	15		0.05			0.05		0.05	
V_{IH}	Input high* voltage			0.5/4.5	<1	5	3.5		3.5			3.5		V
				1/9	<1	10	7		7			7		
				1.5/13.5	<1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	<1	5		1.5			1.5		1.5	V
				9/1	<1	10		3			3		3	
				13.5/1.5	<1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.
The Noise Margin for both "1" and "0" level is:

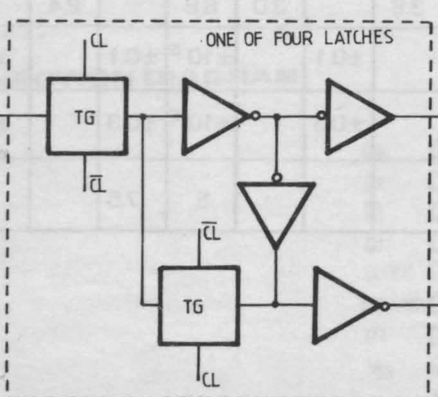
1 V min. with $V_{DD} =$ 5 V
2 V min. with $V_{DD} =$ 10 V
2.5 V min. with $V_{DD} =$ 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ k, typical temperature coeficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

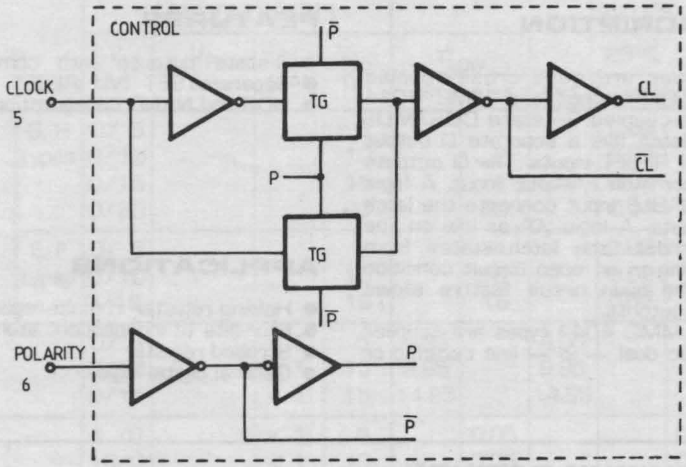
	Parameter		Test conditions V_{DD}(V)	Values Min.	Values Typ.	Values Max.	Unit
t_{PLH}, t_{PHL}	Propagation delay time	Data In to Q	5 10 15		110 55 40	220 110 80	ns
		Data In to $\overline{Q}$	5 10 15		150 75 50	300 150 100	ns
		Clock to Q	5 10 15		225 100 80	450 200 160	ns
		Clock to $\overline{Q}$	5 10 15		225 115 90	450 230 180	ns
t_{THL}, t_{TLH}	Transition time		5 10 15		100 50 40	200 100 80	ns
t_W,	Clock pulse width		5 10 15	200 100 60	100 50 30		ns
t_{setup},	Setup time		5 10 15	50 30 25	0 0 0		ns
t_{hold},	Hold time		5 10 15	120 60 50	60 30 25		ns
t_r, t_f,	Clock input rise and fall time		5 10 15	Not rise or fall time sensitive			ns

LOGIC DIAGRAM



TRUTH TABLE

CLOCK	POLARITY	Q
0	0	D
	0	LATCH
1	1	D
	1	LATCH


CONTROL
CLOCK
5
TG
TG
P
P̄
CL
C̄L̄
POLARITY
6

QUAD 3-STATE R/S LATCHES:
QUAD NOR R/S LATCH-MMC 4043
QUAD NAND R/S LATCH-MMC 4044

GENERAL DESCRIPTION

The MMC 4043 types are quad cross-coupled 3-state COS/MOS NOR latches and MMC 4044 types are quad cross-coupled 3—state COS/MOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic „1" or high on the ENABLE input connects the latch states to the Q outputs. A logic „0" or low on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common busing of the outputs.
The MMC 4043 and MMC 4044 types are supplied in 16 — lead hermetic dual — in — line ceramic or plastic packages.

FEATURES

- 3-state outputs with common output ENABLE
- Separate SET and RESET inputs for each latch
- NOR and NAND configurations

APPLICATIONS

- Holding register in multi-register system
- Four-bits of independent storage with output enable
- Strobed register
- General digital logic

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			± 10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Imput voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM

MMC 4043

Q4	1	16	V_{DD}
Q1	2	15	R4
R1	3	14	S4
S1	4	13	NC
ENABLE	5	12	S3
S2	6	11	R3
R2	7	10	Q3
V_{SS}	8	9	Q2

MMC 4044

Q4	1	16	V_{DD}
NC	2	15	S4
S1	3	14	R4
R1	4	13	Q1
ENABLE	5	12	R3
R2	6	11	S3
S2	7	10	Q3
V_{SS}	8	9	Q2

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
I_{OH}	3—state output	G, H types	0/18	0/18		18		±0.4		$\pm 10^{-4}$	±0.4		±12	μA
		E, F types	0/15	0/15		15		±1.0		$\pm 10^{-4}$	±1.0		±7.5	

PARAMETER		TEST CONDITIONS				VALUES							UNIT
		V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
						min.	max.	min.	typ	max.	min.	max.	
C_I	Input capacitance		Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

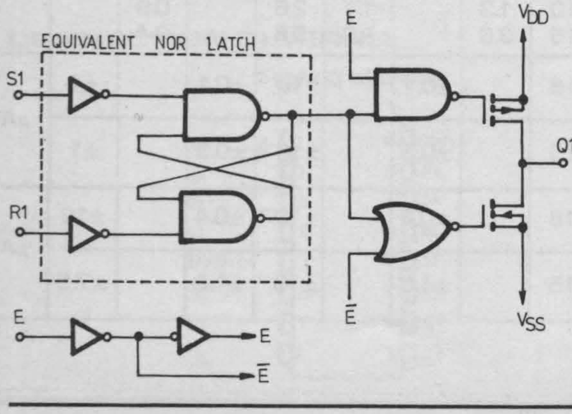
DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, input t_r, t_r = 20ns, C_L = 50 pF, R_L = 200 kΩ)

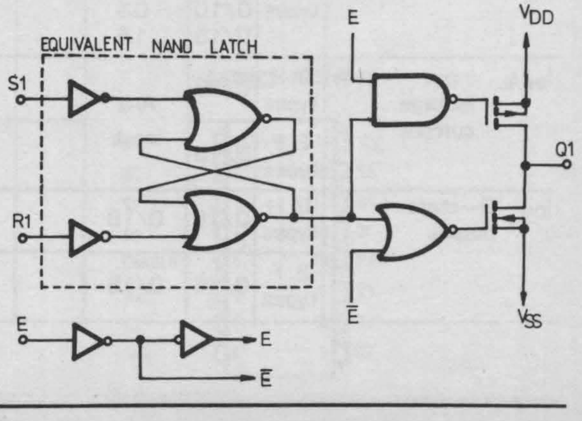
PARAMETER		V_{DD} (V)	VALUES typ.	VALUES max.	UNITS
t_{PLH} t_{PHL}	Propagation delay time (SET or RESET to Q)	5 10 15	150 70 50	300 140 100	ns
t_{PHZ} t_{PZH}	3-state propagation delay time (ENABLE to Q)	5 10 15	115 55 40	230 110 80	ns
t_{PLZ} t_{PZL}	3-state propagation delay time	5 10 15	90 50 35	180 100 70	ns
t_{THL} t_{TLH}	Transition time	5 10 15	100 50 40	200 100 80	ns
t_w	SET or RESET pulse width	5 10 15	80 40 20	160 80 40	ns

LOGIC DIAGRAMS

MMC 4043

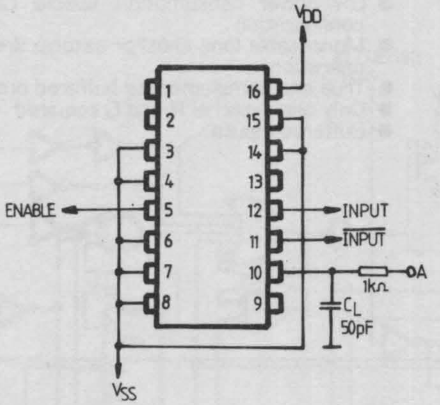


MMC 4044



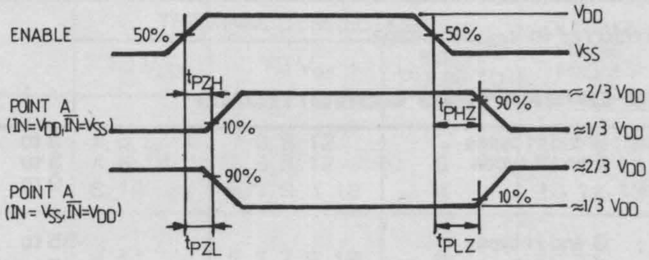
TEST CIRCUITS

ENABLE propagation delay time and waveforms



TEST	IN	$\overline{IN}$	A
t_{PHZ}	V_{DD}	V_{SS}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}	V_{DD}
t_{PZH}	V_{DD}	V_{SS}	V_{SS}
t_{PZL}	V_{SS}	V_{DD}	V_{DD}

Z = HIGH IMPEDANCE



LOW-POWER MONOSTABLE/ ASTABLE MULTIVIBRATOR

GENERAL DESCRIPTION

The MMC 4047 is a monolithic integrated circuit processed in standard Al-gate CMOS technology available in 14 lead dual in-line package. The MMC 4047 consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options. Inputs include +TRIGGER,-TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER and EXTERNAL RESET. Buffered outputs are Q,$\overline{Q}$ and OSCILLATOR. In all modes of operation, an external capacitor must be connected between C-Timing and C-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals.

FEATURES

- Low-power consumption: special CMOS oscillator configuration
- Monostable (one-shot) or astable (free-runing) operation
- True and complemented buffered outputs
- Only one external R and C required
- Buffered inputs

ABSOLUTE MAXIMUM RATINGS

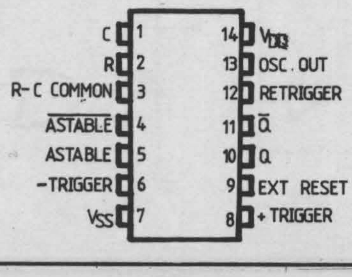
V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_i	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		±10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

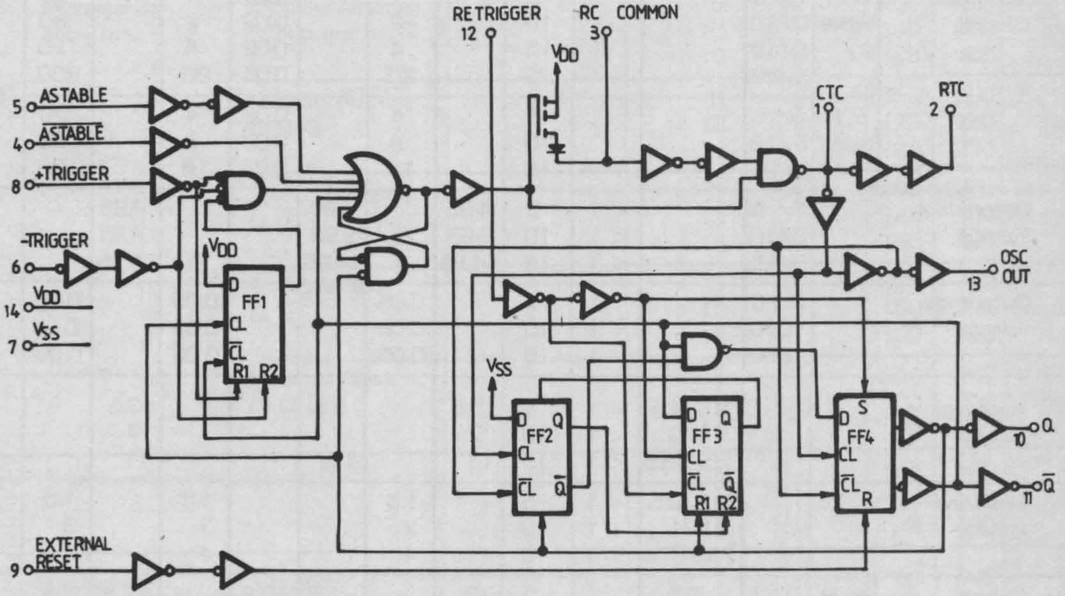
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_i	Imput voltage	0 to	V_{DD}	V
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



LOGIC DIAGRAM



FUNCTIONAL TERMINAL CONNECTIONS

FUNCTION*	TERMINAL CONNECTIONS TO V_{DD}	TERMINAL CONNECTIONS TO V_{SS}	INPUT PULSE TO	OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
Astable multivibrator:					
Free running	4, 5, 6, 14	7, 8, 9, 12	—	10,11, 13	t_A(10, 11)=4.40 RC
True gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	t_A(13)=2.20 RC
Complement gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	
Monostable multivibrator:					
Positive-edge trigger	4, 14	5, 6, 7, 9, 12	8	10, 11	
Negative-edge trigger	4, 8, 14	5, 7, 9, 12	6	10, 11	
Retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	t_M(10, 11)=2.48 RC
External countdown**	14	5, 6, 7, 8, 9, 12	—	10, 11	

* In all cases external capacitor and resistor between pins 1, 2 and 3 (see logic diagrams)

** Input pulse to reset of external counting chip.
External counting chip output to pin 4

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V

2 V min. with $V_{DD} = 10$ V

2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 15 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

	PARAMETER		TEST CONDITIONS V_{DD} (V)	VALUES min.	VALUES typ.	VALUES max.	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	Astable, $\overline{\text{Astable}}$ to osc. out	5 10 15		200 100 80	400 200 160	ns
		Astable, $\overline{\text{Astable}}$ to Q, $\overline{\text{Q}}$	5 10 15		350 175 125	700 350 250	ns
		+ or − Trigger to Q, $\overline{\text{Q}}$	5 10 15		500 225 150	1000 450 300	ns
		Retrigger to Q, $\overline{\text{Q}}$	5 10 15		300 150 100	600 300 200	ns
		External Reset to Q, $\overline{\text{Q}}$	5 10 15		250 100 70	500 200 140	ns
t_{THL}, t_{TLH}	Transition time osc. out Q, $\overline{\text{Q}}$		5 10 15		100 50 40	200 100 80	ns
t_W	Input pulse width:	+Trigger, −Trigger	5 10 15		200 80 50	400 160 100	ns
		Reset	5 10 15		100 50 30	200 100 60	ns
		Retrigger	5 10 15		300 115 75	600 230 150	ns
t_r, t_f	Input rise and fall time All inputs		5 10 15		Unlimited		μs
	Q or $\overline{\text{Q}}$ deviation from 50% Duty factor		5 10 15		±0.5 ±0.5 ±0.1	±1 ±1 ±0.5	%

APPLICATION INFORMATION

1 - Circuit description

Astable operation is enabled by a high level on the ASTABLE input. The period of the square wave at the Q and $\overline{\text{Q}}$ Outputs in this mode of operation is a function of the external components employed. „True" input pulses on the ASTABLE input or „Complement" pulses on the $\overline{\text{ASTABLE}}$ input alow the circuit to be used as a gatable multivibrator. The OSCILLATOR output period will be half of the Q terminal output in the astable mode. However, a 50% duty cycle is not guaranteed at this output. In the monostable mode, positive-edge triggering is accomplished by application of a leading-edge pulse to the +TRIGER input and a low level to the −TRIGGER input. For negative-edge triggering, a trailing-edge pulse is applied to the −TRIGGER and a high level is applied to the +TRIGGER. Input pulses may be of any duration relative to the output pulse.

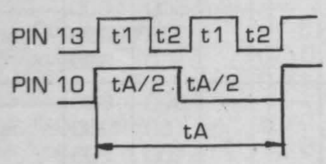
The multivibrator can be retriggered (on the leading edge only) by applying a common pulse to both the RETRIGGER and +TRIGGER inputs. In this mode the output pulse remains high as long as the input pulse period is shorter than the period determined by the RC components. An external countdown option can be implemented by coupling „Q" to an external „N" counter and resetting the counter with the trigger pulse. The

counter output pulse is fed back to the $\overline{\text{ASTABLE}}$ input and has a duration equal to N times the period of the multivibrator. A high level on the EXTERNAL RESET input assures no output pulse during an „ON" power condition. This input can also be activated to terminte the output pulse at any time. In the monostable mode, high-level or power-on reset pulse, must be applied to the EXTERNAL RESET whenever V_{DD} is applied.

2 - Astable Mode

The following anlysis presents worst-case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift (33%—67% V_{DD}) for free-running (astable) operation.

Astable mode waveforms



$$t1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_{TR}}$$

$$t2 = -RC \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}}$$

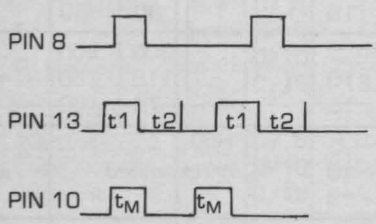
$$t_A = 2(t1 + t2) = -2RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} - V_{TR})(2V_{DD} - V_{TR})}$$

Typ: $V_{TR} = 0.5\ V_{DD}$ $t_A = 4.40$ RC
Min: $V_{TR} = 0.33\ V_{DD}$ $t_A = 4.62$ RC
Max: $V_{TR} = 0.67\ V_{DD}$ $t_A = 4.62$ RC
thus if $t_A = 4.40$ RC is used, the maximum variation will be (+5.0%, − 0.0%) In addition to variations from unit-to-unit, the astable period may vary as a function of frequency with respect to V_{DD} and temperature.

3 - Monostable Mode

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift (33%—67% V_{DD}) for one-shot (monostable) operation.

Monostable waveforms



$$t1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_{DD}}$$

$$t2 = -RC \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}}$$

$$tM = (t1 + t2) = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2V_{DD} - V_{TR})(2V_{DD})}$$

where t_M = monostable mode pulse width. Values for t_M are as follows:
Typ: $V_{TR} = 0.5\ V_{DD}$ $t_M = 2.48$ RC
Min: $V_{TR} = 0.33\ V_{DD}$ $t_M = 2.71$ RC
Max: $V_{TR} = 0.67\ V_{DD}$ $t_M = 2.48$ RC
Thus if $t_M = 2.48$ RC is used, the maximum variation will be (+9.3% − 0.0%)

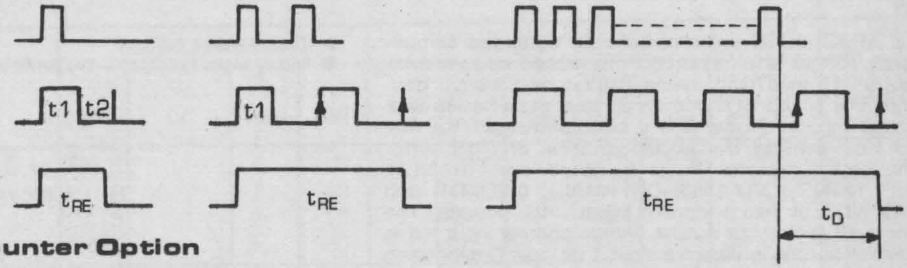
Note: In the astable mode the first positive half cycle has a duration of T_M; succeding durations are $t_A/2$. In addition to variations from unit-to-unit, the monostable pulse width may vary as a function of frequency with respect to V_{DD} and temperature.

4 - Retrigger mode

The MMC 4047 can be used in the retrigger mode to extend the output-pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminals 8 and 12, and the output is taken from terminal 10 or 11. As shown in Fig. A normal monostable action is obtained when one retrigger pulse is applied. For two input pulses, $t_{RE} = t_1 + t_1 + 2t_2$.

For more than two pulses, t_{RE}(Q OUTPUT) terminates at some variable time t_D after the termination of the last retrigger pulse. t_D is variable because t_{RE}(Q OUTPUT) terminates after the second positive edge of the oscillator output appears at flip-flop 4 (see logic diagram).

Fig. A` Retrigger-mode waveforms



5-External Counter Option

Time t_M can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration small timing capacitors for long time periods and extremely fast recovery time.
A typical implementation is shown in Fig. B. The pulse duration at the output is

$$t_{ext} = (N-1)t_A + (t_M + t_A/2)$$

where t_{ext} = pulse duration of the circuitry, and N is the number of counts used.

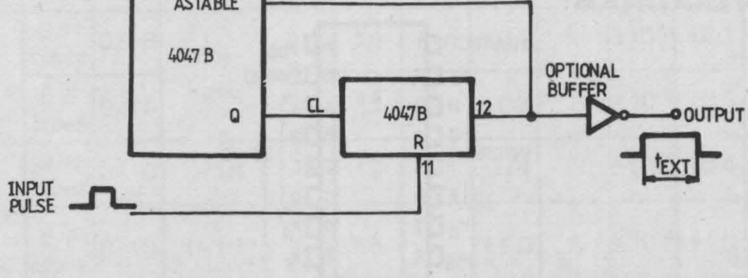
6-Power Consumption

In the standby mode (Monostable or Astable), power dissipation will be a function of leakage current in the circuit, as shown in the static electrical characteristics. For dynamic operation, the power needed to charge the external timing capacitor C is given by the following formula:
Astable Mode: $P = 2CV^2f$. (Output at Pin 13)
$P = 4CV^2f$. (Output at Pin 10 and 11)
Monostable Mode: $P = (1/T)\ (2.9\ CV^2)$ (Duty Cycle). (Output at Pin 10 and 11) The circuit is designed so that most of the total power is consumed in the external components. In practice, the lower the values of frequency and voltage used, the closer the actual power dissipation will be to the calculated value.
Because the power dissipation does not depend on R, a design for minimum power dissipation would be a small value of C. The value of R would depend on the desired period (within the limitations discussed above).

7 - Timing-component limitations

The capacitor used in the circuit should be non-polarized and have low leakage (i.e. the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used). There is no upper or lower limit for either R or C value to maintain oscillation. However, in consideration of accuracy, C must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R must be much larger than the CMOS "ON" resistance in series with it, which typically is hundreds of ohms. In addition, with very large values of R, some short-term instability with respect to time may be noted.
The reccomended values for these components to maintain agreement with previously calculated formulas without trimming should be:
$C \geq 100$ pF, up to any practical value, for astable modes;
$C \geq 1000$ pF, up to any practical value, for monostable modes. $10k \leq R \leq 1M$.

Fig. B` Implementation of external counter option



MULTIFUNCTION EXPANDABLE 8-INPUT GATE

GENERAL DESCRIPTION

The MMC 4048 (intermediate or extended temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package. The MMC 4018 is an 8-input gate having four control inputs. Three binary control inputs` Ka, Kb, and Kc` provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR and AND/NOR. A fourth control input` Kd` provides the user with a 3-state output. When control input Kd is high the output is either a logic 1 or logic 0 depending on the inner states. When control input Kd is low, the output is an open circuit. This feature enables the user to connect this device to a common bus line. In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs to one MMC 4048. For example, two MMC 4048 can be cascaded to provide a 16-input multifunction gate. When the EXPAND input is not used, it should be connected to V_{SS}.

FEATURES

- Three-state output
- Many logic functions available in one package.

ABSOLUTE MAXIMUM RATINGS

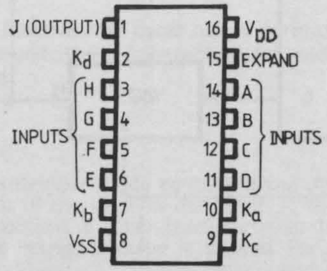
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Imput voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
		E, F types	0/ 5			5		1		0.01	1		7.5	
			0/10			10		2		0.01	2		15	
			0/15			15		4		0.01	4		30	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15	Any input		15		±0.3		$\pm10^{-5}$	±0.3		±1	
I_{OH}	3—state output	G, H types	0/18	0/18		18		±0.4		$\pm10^{-4}$	±0.4		±12	μA
		E, F types	0/15	0/15		15		±1.0		$\pm10^{-4}$	±1.0		±7.5	

PARAMETER	TEST CONDITIONS				VALUES							UNIT
	V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
					min.	max.	min.	typ	max.	min.	max.	
C_I — Input capacitance		Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

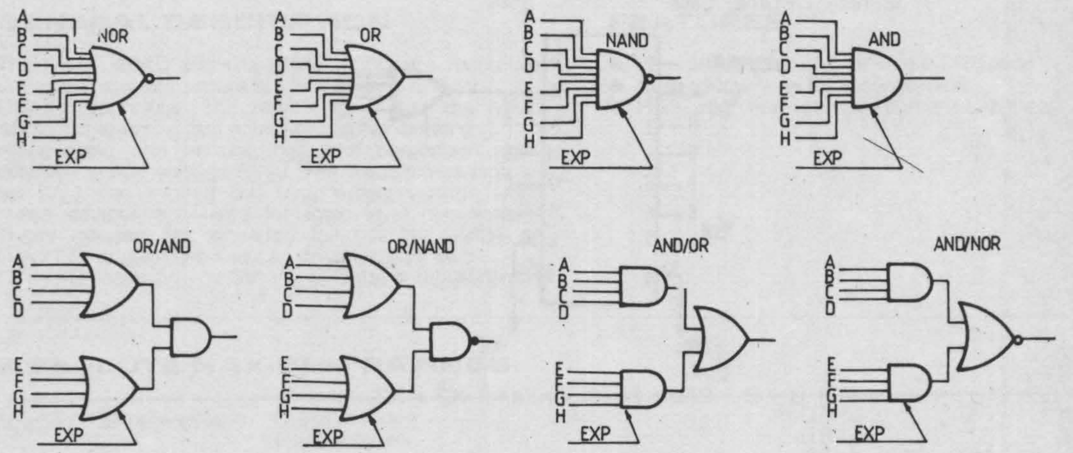
($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kohm, typical temperature coefficient for all $V_{DD} = 0.3\%/°C$ values, all input rise and fall time = 20 ns)

PARAMETER		TEST CONDITIONS		VALUES			UNIT
			V_{DD} (V)	min.	typ.	max.	
t_{PHL}, t_{PLH}	Propagation delay time Inputs to output and Ka to Output		5 10 15		300 150 120	600 300 240	ns
	Kb to Output		5 10 15		225 85 55	450 170 110	ns
	Kc to Output		5 10 15		140 50 40	280 100 80	ns
	Expand Input to Output		5 10 15		190 90 65	380 180 130	ns
t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL}	3-state propagation delay time Kd to Output	$R_L = 1$ k	5 10 15		80 35 25	160 75 50	ns
t_{THL}, t_{TLH}	Transition time		5 10 15		100 50 40	200 100 80	ns
3-state output capacitance					5	10	pF

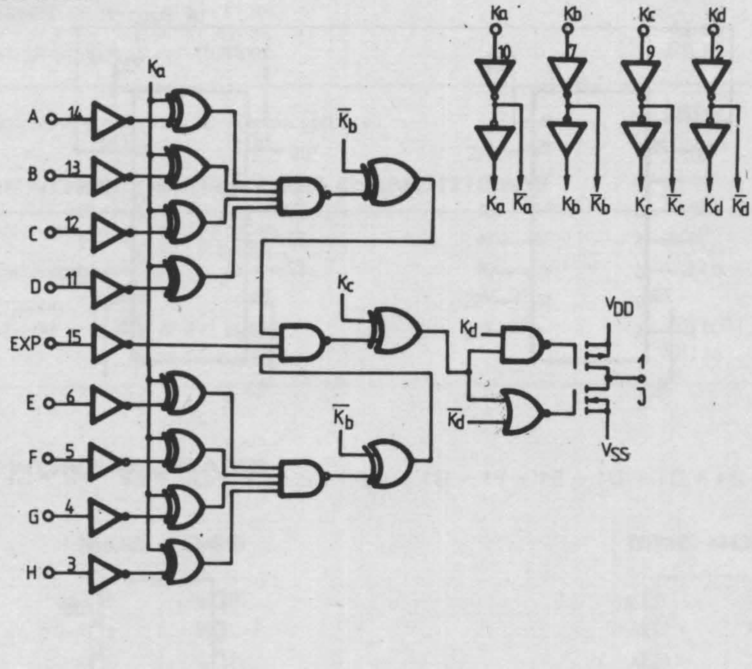
FUNCTION TRUTH TABLE

OUTPUT FUNCTION	BOOLEAN EXPRESION	Ka	Kb	Kc	UNUSED INPUT
NOR	$J = \overline{A+B+C+D+E+F+G+H}$	0	0	0	V_{SS}
OR	$J = A+B+C+D+E+F+G+H$	0	0	1	V_{SS}
OR/AND	$J = (A+B+C+D) \cdot (E+F+G+H)$	0	1	0	V_{SS}
OR/NAND	$J = \overline{(A+B+C+D) \cdot (E+F+G+H)}$	0	1	1	V_{SS}
AND	$J = ABCDEFGH$	1	0	0	V_{DD}
NAND	$J = \overline{ABCDEFGH}$	1	0	1	V_{DD}
AND/NOR	$J = \overline{ABCD + EFGH}$	1	1	0	V_{DD}
AND/OR	$J = ABCD + EFGH$	1	1	1	V_{DD}
Kd = 1 Normal Inverter Action Kd = 0 High Impedance Output					
EXPAND Input = o					

BASIC LOGIC CONFIGURATIONS

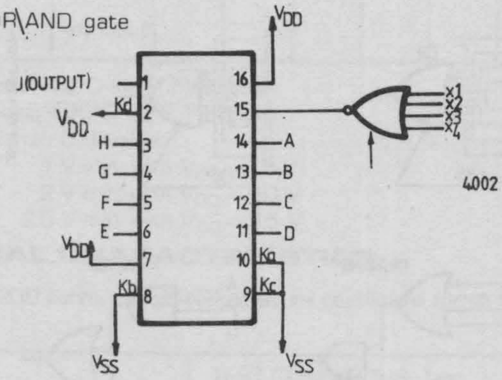


LOGIC DIAGRAM



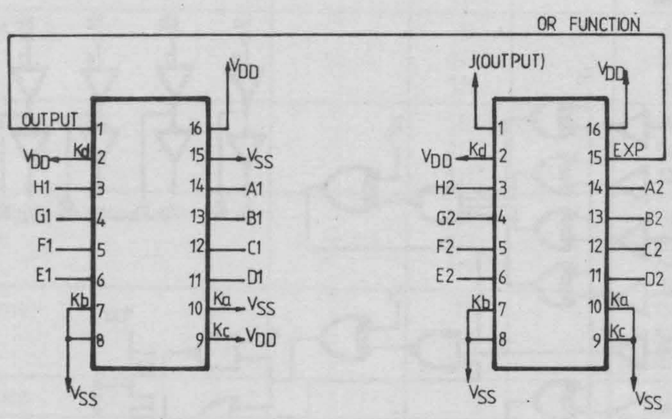
APPLICATIONS

12-input OR\AND gate



J = (A + B + C + D)(E + F + G + H)(X1 + X2 + X3 + X4)

16 - INPUT NOR GATE



J = A1 + B1 + C1 + D1 + E1 + F1 + G1 + A2 + B2 + C2 + D2 + E2 + F2 + G2 + H2

HEX BUFFER/CONVERTERS: MMC 4049-INVERTING TYPE MMC 4050-NON-INVERTING TYPE

GENERAL DESCRIPTION

The MMC 4049 and the MMC 4050 are monolithic integrated circuits processed in standard Al-gate CMOS technology. The MMC 4049 and the MMC 4050 are inverting and non-inverting hex-buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{DD}). The input-signal high level (V_{IH}) can exceed the V_{DD} supply voltage when these devices are used for logic level conversions. These devices are intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads ($V_{DD} = 5V$, $V_{OL} \leqslant 0.4V$, and $I_{OL} \geqslant 3.2mA$).

FEATURES

- High sink current for driving 2TTL loads
- High-to-low level logic conversion
- High sink and source current capability

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

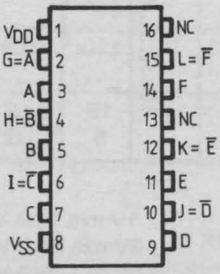
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

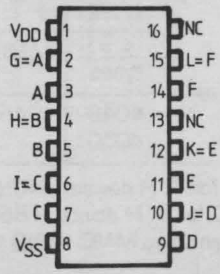
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Imput voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAMS

MMC 4049



MMC 4050



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5		5		1		0.02	1		30	μA
			0/10		10		2		0.02	2		60	
			0/15		15		4		0.02	4		120	
			0/20		20		20		0.04	20		600	
		E, F types	0/ 5		5		4		0.02	4		30	
			0/10		10		8		0.02	8		60	
			0/15		15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		5	4.95		4.95			4.95		V
			0/10		10	9.95		9.95			9.95		
			0/15		15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		5		0.05			0.05		0.05	V
			10/0		10		0.05			0.05		0.05	
			15/0		15		0.05			0.05		0.05	
V_{IH}	Input high voltage (4049)			0.5	5	4		4			4		V
				1	10	8		8			8		
				2	15	12		12			12		
V_{IH}	Input high voltage (4050)			4.5	5	3.5		3.5			3.5		V
				9	10	7		7			7		
				13.5	15	11		11			11		
V_{IL}	Input low voltage (4049)			4.5	5		1			1		1	V
				9	10		2			2		2	
				13	15		3			3		3	
V_{IL}	Input low voltage (4050)			0.5	5		1.5			1.5		1.5	V
				1	10		3			3		3	
				1.5	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5	5	1.6		-1.25	-6.4		-0.9		mA
			0/ 5	4.6	5	0.64		-0.51	-1.6		-0.36		
			0/10	9.5	10	1.6		-1.30	-3.6		-0.9		
			0/15	13.5	15	4.7		-3.75	-12		-2.6		
		E, F types	0/ 5	2.5	5	1.5		-1.25	-6.4		-1		
			0/ 5	4.6	5	0.61		-0.51	-1.6		-0.42		
			0/10	9.5	10	1.5		-1.25	-3.6		-1		
			0/15	13.5	15	4.5		-3.75	-12		-3		
I_{OL}	Output sink current	G, H types	0/ 5	0.4	5	3.75		3.2	6.4		2.2		
			0/10	0.5	10	10		8	16		5.6		
			0/15	1.5	15	30		24	48		17		
		E, F types	0/ 5	0.4	5	3.6		3.2	6.4		2.6		
			0/10	0.5	10	9.6		8	16		6.6		
			0/15	1.5	15	28		24	48		19		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15		15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance	4049	Any input						15	22.5			pF
		4050							5	7.5			

* $T_{LOW} = -55°C$ for G, H device: $-40°C$ for E, F device

* $T_{HIGH} = +125°C$ for G, H device: $+85°C$ for E, F device

The noise margin (only MMC 4050 type) for both „1" and „0" level is:

1V min. with $V_{DD} = 5V$

2V min. with $V_{DD} = 10V$

2.5V min. with $V_{DD} = 15V$

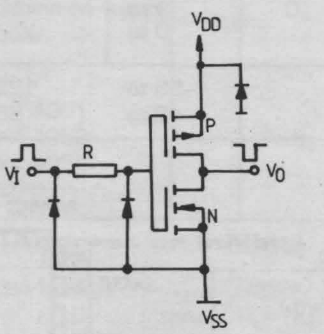
DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns).

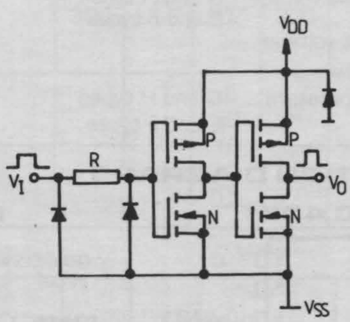
PARAMETER		TEST CONDITIONS		VALUES			UNIT
		V_I(V)	V_{DD}(V)	min.	typ.	max.	
t_{PLH}	Propagation delay time (4049)	5	5		60	120	ns
		10	10		32	65	
		10	5		45	90	
		15	15		25	50	
		15	5		45	90	
t_{PLH}	Propagation delay time (4050)	5	5		70	140	ns
		10	10		40	80	
		10	5		45	90	
		15	15		30	60	
		15	5		40	80	
t_{PHL}	Propagation delay time (4049)	5	5		32	65	ns
		10	10		20	40	
		10	5		15	30	
		15	15		15	30	
		15	5		10	20	
t_{PHL}	Propagation delay time (4050)	5	5		55	110	ns
		10	10		22	55	
		10	5		50	100	
		15	15		15	30	
		15	5		50	100	
t_{TLH}	Transition time	5	5		80	160	ns
		10	10		40	80	
		15	15		30	60	
t_{THL}	Transition time	5	5		30	60	ns
		10	10		20	40	
		15	15		15	30	

SCHEMATIC DIAGRAMS

MMC 4049



MMC4050



ANALOG MULTIPLEXERS-DEMULTIPLEXERS:

SINGLE 8-CHANNEL
DIFFERENTIAL 4-CHANNEL
TRIPLE 2-CHANNEL

GENERAL DESCRIPTION

The MMC 4051, MMC 4052 and MMC 4053 are monolithic integrated circuits, available in 16-lead dual-in-line plastic or ceramic package. MMC 4051, MMC 4052 and MMC 4053 analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance and very low OFF leakage current. These multiplexer circuits dissipate extremely low quiescent power over the full V_{DD}—V_{SS} and V_{DD}—V_{EE} supply-voltage ranges, independent of the logic state of the control signals. When a-logic „1" is present at the inhibit input terminal all channel are off. The MMC 4051 is a single 8-channel multiplexer having three binary control inputs, A, B and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output. The MMC 4052 is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs. The MMC 4053 is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a singlepole double-throw configuration.

FEATURES

- Low „ON" resistance: 125 ohm (typ.) over 15 Vp.p. signal-input range for $V_{DD}—V_{EE} = 15$ V
- High „OFF" resistance: channel leakage ± 100 pA (typ.) $V_{DD}—V_{EE} = 18$ V
- Binary address decoding on chip
- Very low quiescent power dissipation under all digital control input and supply conditions: 0.2/uW (typ.), $V_{DD}—V_{SS} = V_{DD}—V_{EE} = 10$ V
- Matched switch characteristics: $R_{ON} = 5$ ohm (typ.) for $V_{DD}—V_{EE} = 15$ V
- Wide range of digital and analog signal levels: digital 3 to 20 V, analog to 20 Vp.p.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

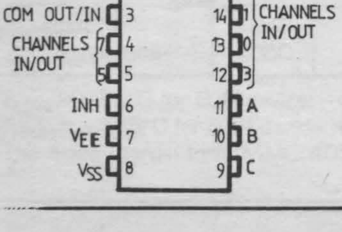
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

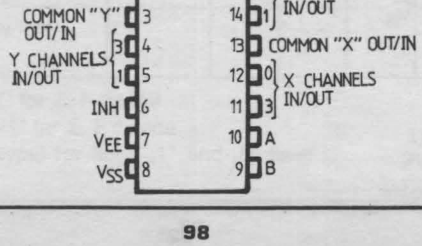
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAMS

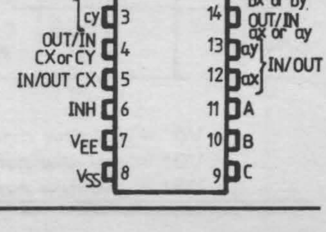
MMC 4051



MMC 4052



MMC 4053



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		Test conditions V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ.	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L quiescent device current	G, H types				5		5		0.04	5		150	
					10		10		0.04	10		300	
					15		20		0.04	20		600	
					20		100		0.08	100		3000	
	E, F types				5		20		0.04	20		150	
					10		40		0.04	40		300	µA
					15		80		0.04	80		600	

Switch

PARAMETER			Test conditions V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ.	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
ON-resistance		G, H types	$0 \le V_I \le V_{DD}$	0	0	5		880		470	1050		1200	
			$0 \le V_I \le V_{DD}$	0	0	10		310		180	400		580	
			$0 \le V_I \le V_{DD}$	0	0	15		220		125	280		400	
		E, F types	$0 \le V_I \le V_{DD}$	0	0	5		880		470	1050		1200	Ω
			$0 \le V_I \le V_{DD}$	0	0	10		330		180	400		520	
			$0 \le V_I \le V_{DD}$	0	0	15		230		125	280		360	
ΔON-resistance (between any 2 channels)				0	0	5				10				
				0	0	10				10				Ω
				0	0	15				5				
OFF (●) channel leakage current	Any channel OFF	G, H types		0	0	18		100		±0.1	100		1000	nA
	All channels OFF (common OUT/IN)	G, H types		0	0	18		100		±0.1	100		1000	nA
	Any channel OFF	E, F types		0	0	15		300		±0.1	300		1000	nA
	All channels OFF (common OUT/IN)	E, F types		0	0	15		300		±0.1	300		1000	nA
C-capacitance	Input			−5	−5	5				5				
	Output 4051			−5	−5	5				30				
	Output 4052			−5	−5	5				18				pF
	Output 4053			−5	−5	5				9				
	Feedthrough			−5	−5	5				0.2				

Control (Address or Inhibit)

PARAMETER		Test conditions		V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ.	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
V_{IL}	Input low voltage	$= V_{DD}$ thru 1KΩ	$V_{EE} = V_{SS}$ R_L=1KΩ to V_{SS}	5		1.5			1.5		1.5	
		$= V_{DD}$ thru 1KΩ	$V_{EE} = V_{SS}$ R_L=1KΩ to V_{SS}	10		3			3		3	V
		$= V_{DD}$ thru 1KΩ	$V_{EE} = V_{SS}$ R_L=1KΩ to V_{SS}	15		4			4		4	
V_{IH}	Input high voltage	$= V_{DD}$ thru 1KΩ	$I_{IS} > 2\mu A$ (on all OFF channels)	5	3.5		3.5			3.5		
		$= V_{DD}$ thru 1KΩ	$I_{IS} > 2\mu A$ (on all OFF channels)	10	7		7			7		V
		$= V_{DD}$ thru 1KΩ	$I_{IS} > 2\mu A$ (on all OFF channels)	15	11		11			11		

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ.	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_{IH}, I_{IL} Input leakage current	G, H types	$V_I = 0/18$ V			18		±0.1		$\pm10^{-3}$	±0.1		±1	μA
	E, F types	$V_I = 0/15$ V			15		±0.3		$\pm10^{-3}$	±0.3		±1	μA
C_I Input capacitance		Any address or inhibit input							5	7.5			pF

(o) Determined by minimum feasible leakage measurement for automatic testing
(*) $T_{Low} = -55°C$ for G, H device; $-40°C$ for E, F device.
$T_{High} = +125°C$ for G, H device; $+85°C$ for E, F device.

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, all input square wave rise and fall time = 20 ns)

PARAMETER	TEST CONDITIONS V_{EE} (V)	R_L (KΩ)	f_i (KHz)	V_{IS} (V)	V_{SS} (V)	V_{DD} (V)			VALUES typ.	max.	UNIT
Switch											
t_{pd}-Propagation delay time (Signal Input to output)		200		10 V (pulse)		5 10 15			30 15 11	30 60 20	ns
Frequency response channel „ON" (Sine wave Input) at $20 \text{ Log } \frac{V_O}{V_I} = -3$ dB	$=V_{SS}$	1		5(•)		10	VO at common OUT/IN	4053 4052 4051	30 25 20		MHz
							V_O at any channel		60		MHz
Feedthrough (all channels OFF) at $20 \text{ Log } \frac{V_O}{V_1} = -40$ dB	$=V_{SS}$	1		5(•)		10	V_O at common OUT/IN	4053 4052 4051	8 10 12		MHZ
							V_O at any channel		8		MHz
Frequency signal crosstalk at $20 \text{ Log } \frac{V_O}{V_I} = -40$ dB	$= V_{SS}$	1		5(•)		10	Between any 2 channels		3		MHz
							Between sections 4052 only	Measured on common	6		MHz
								Measured on any channel	10		MHz
							Between any 2 sections 4053 only	In pin 2 out pin 14	2.5		MHz
								In pin 15 out pin 14	6		MHz
Sine wave distortion $f_{IS} = 1$ KHz sine wave	$=V_{SS}$	10 10 10	1 1 1	2(•) 3(•) 5(•)		5 10 15			0.3 0.2 0.12		%

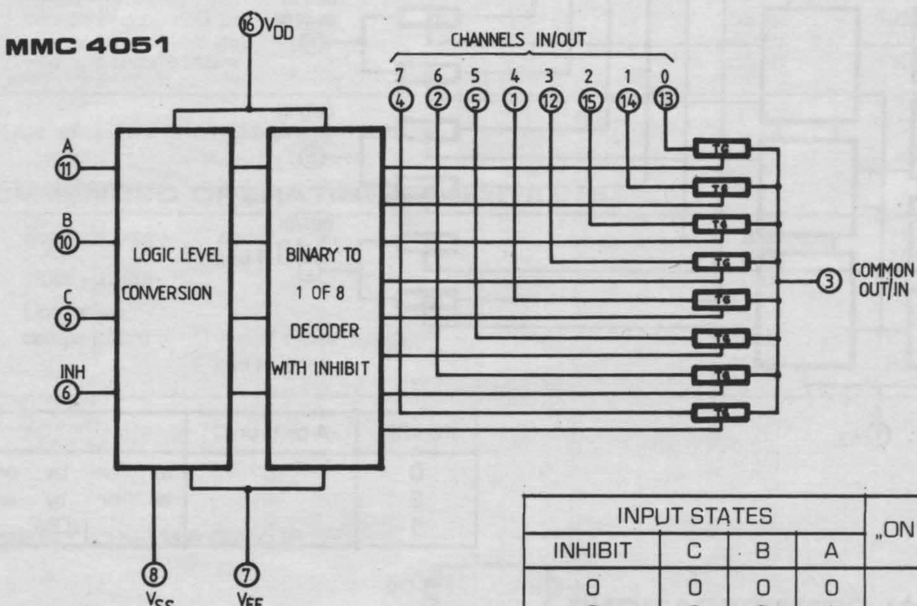
PARAMETER	TEST CONDITIONS							VALUES		UNIT
	V_{EE} (V)	R_L (K)	f_i (KHz)	V_{IS} (V)	V_{SS} (V)	V_{DD} (V)		typ.	max.	
Control (address or inhibit)										
Propagation delay time: Address-to signal OUT channels ON or OFF	0 0 0 – 5				0 0 0 0	5 10 15 5		360 160 120 225	720 320 240 450	ns
Propagation delay time: Inhibit to signal OUT (channel turning ON)	0 0 0 – 10	10			0 0 0 0	5 10 15 5		360 160 120 200	720 320 240 400	ns
Propagation delay time: Inhibit to signal OUT (channel turning OFF)	0 0 0 – 10	0.3				5 10 15 5		200 90 70 130	450 210 160 300	ns
Address or inhibit to signal crosstalk	0	10(✳)			0	10	$V_C = V_{DD} - V_{SS}$ (Square wave)	65		mV peak

(●) Peak to peak voltage symetrical about $\frac{V_{DD} - V_{EE}}{2}$

(✳) Both ends of channel.

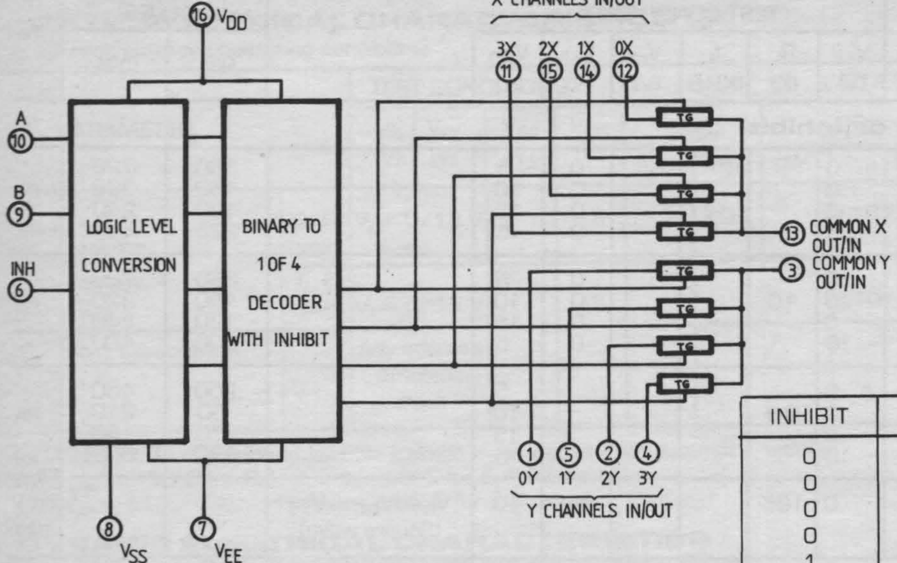
FUNCTIONAL DIAGRAMS AND TRUTH TABLES

MMC 4051



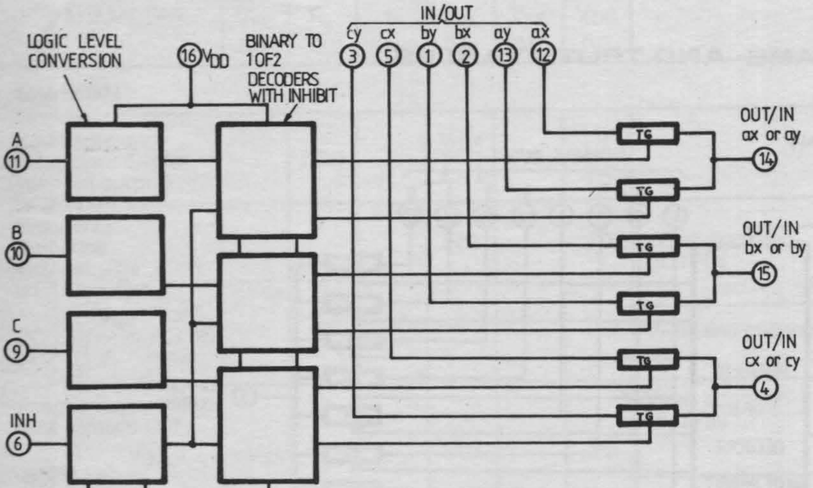
INPUT STATES				„ON" CHANNEL(S)
INHIBIT	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	NONE

MMC 4052



INHIBIT	B	A		
0	0	0	0x,	0y
0	0	1	1x,	1y
0	1	0	2x,	2y
0	1	1	3x,	3y
1	X	X	NONE	

MMC 4053



INHIBIT	A or B or C					
0	0	ax	or	bx	or	cx
0	1	ay	or	by	or	cy
1	X	NONE				

SPECIAL CONSIDERATIONS

Control of analog signals up to 20 V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20 V (if $V_{DD}-V_{SS} = 3$ V, a $V_{DD}-V_{EE}$ of up to 13 V can be controlled; for $V_{DD}-V_{EE}$ level differences above 13 V, a $V_{DD}-V_{SS}$ of at least 4.5V is required). For example, if $V_{DD} = +5$V, $V_{SS} = 0$, and $V_{EE} = -13.5$V, analog signals from -13.5V to $+4.5$V can be controlled by digital inputs of 0 to 4.5V. In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt. No V_{DD} current will flow through R_L if the switch current flows into lead 3 on the MMC 4051; leads 3 and 13 on the MMC 4052; leads 4, 14, 15 on the MMC 4053.

14-STAGE RIPPLE-CARRY BINARY COUNTER/ DIVIDER AND OSCILLATOR

GENERAL DESCRIPTION

The MMC 4060 is a monolithic i.c. processed in standard Al-gate CMOS technology. This device consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of $\emptyset_I$ (and $\emptyset_O$) A high level on the $\overline{RESET}$ line resets the counter to the all O's state and disables the oscillator. Schmitt trigger action on the clock line permits unlimited clock rise and fall times. All inputs and outputs are fully buffered.

FEATURES

- Medium-speed operation
- Fully static operation
- Buffered inputs and outputs
- Common reset

ABSOLUTE MAXIMUM RATINGS

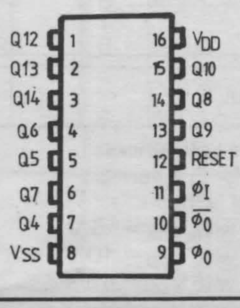
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15	Any input		15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.
The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

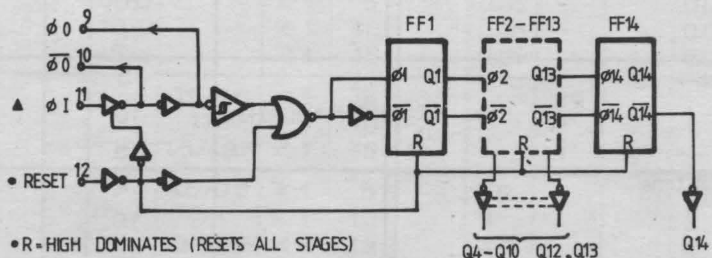
(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20 ns)

PARAMETER		TEST CONDITIONS		VALUES			UNIT
			V_{DD}(V)	Min.	Typ.	Max.	
Input-pulse operation							
t_{PLH}, t_{PHL}	Propagation delay time (Ø to Q4 Out)		5		370	740	ns
			10		150	300	
			15		100	200	
t_{PLH}, t_{PHL}	Propagation delay time (Q_n to Q_{n+1})		5		100	200	ns
			10		50	100	
			15		40	80	
t_{TLH}, t_{THL}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	
t_W	Input pulse width	f = 100 kHz	5		50	100	ns
			10		20	40	
			15		15	30	
t_r, t_f	Input rise and fall time		5	Unlimited			µs
			10				
			15				
f_{max}	Maximum clock input frequency		5	3.5	7		MHz
			10	8	16		
			15	12	24		
Reset operation							
t_{PLH}	Propagation delay time		5		180	360	ns
			10		80	160	
			15		50	100	
t_W	Reset pulse width		5		60	120	ns
			10		30	60	
			15		20	40	
RC operation							
Variation of frequency (Unit-to-Unit)		C_x = 200 pF	5	18	21.5	25	kHz
		R_S = 560 kΩ	10	20	23	26	
		R_x = 50 kΩ	15	21.1	24	27	
Variation of frequency with voltage (Same Unit)		C_x = 200 pF	5V to 10 V	–	–	2	
		R_S = 560 kΩ					
		R_x = 50 kΩ	10 V to 15 V	–	–	1	
R_x max		C_x = 10 µF	5	–	–	20	MΩ
		= 50 µF	10	–	–	20	
		= 10 µF	15	–	–	10	

PARAMETER	TEST CONDITIONS		VALUES			UNIT
		V_{DD}(V)	Min.	Typ.	Max.	
C_x max	R_x = 500 kΩ	5	–	–	1000	μF
	= 300 kΩ	10	–	–	50	
	= 300 kΩ	15	–	–	50	
Maximum Oscillator Frecquency*	R_x = 5 kΩ	10	530	650	810	kHz
	C_x = 15 pF	15	690	800	940	

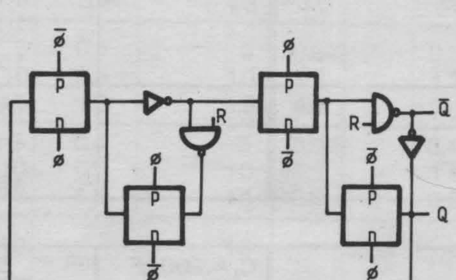
* RC oscillator applications are not recommended at supply voltages below 7 V for R_x = 50 kΩ

LOGIC DIAGRAM



• R = HIGH DOMINATES (RESETS ALL STAGES)
▲ COUNTER ADVANCES ONE BINARY COUNT ON EACH NEGATIVE-GOING TRANSITION OF φI (AND φ0)

Detail of tipical flip-flop stage



QUAD BILATERAL SWITCH FOR TRANSMISSION OR MULTIPLEXING OF ANALOG OR DIGITAL SIGNALS

GENERAL DESCRIPTION

The MMC 4066 (E, F — intermediate temperature range and G, H — extended temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package.

The MMC 4066 is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with MMC 4016, but exhibits a much lower ON resistance. In addition, the ON resistance in relatively constant over the full input-signal range. The MMC 4066 consists of four independent bilateral switches. A single control signal is required per switch. Both the p and n device in a given switch are biased ON or OFF simultaneously by the control signal.

As shown in schematic diagram, the well of the n-channel device on each switch is either tied to the input when the switch is ON or to V_{SS} when the switch is OFF. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the ON resistance low over the full operating-signal range. The advantages over single-channel switches include peak input signal voltage swings equal to the full supply voltage, and more constant ON impedance over the input-signal range.

FEATURES

- 15 V digital or ±7.5 V peak-to-peak switching
- 80 Ω typical ON resistance for 15 V operation
- Switch ON resistance matched to within 5 Ω over 15 V signal-input range
- High on/off output-voltage ratio: 65 dB typ. at f_{is} = 10 kHz, R_L = 10 kΩ
- High degree of linearity: < 0.5% distortion typ at f_{is} = kHz, V_{is} = 5 Vp-p, $V_{DD}—V_{SS} \geq$ 10 V, R_L = 10 kΩ
- Extremely low off switch leakage resulting in very low offset current and high effective OFF resistance; 10 pA typ. at $V_{DD}—V_{SS}$ = 10 V, T_A = 25°C
- Extremely high control input impedance (control circuit solated from signal circuit): 10^{12} Ω typ.
- Low crosstalk between switches: −50 dB typ. at f_{is} = 0.9 MHZ, R_L = 1 k
- Matched control-input to signal-output capacitance: reduces output signal transients

ABSOLUTE MAXIMUM RATINGS

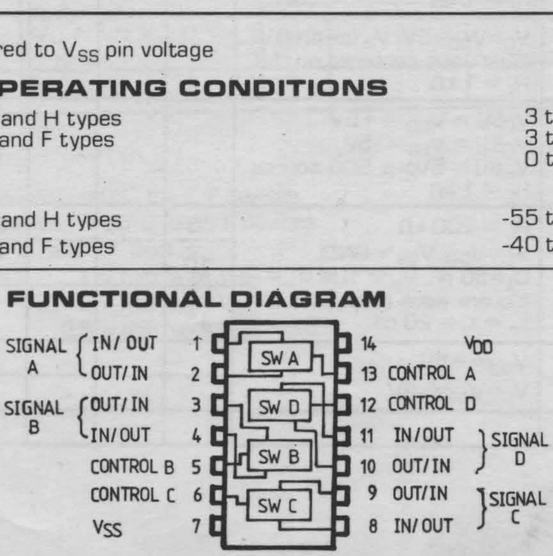
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

FUNCTIONAL DIAGRAM



ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, typical temperature coefficient for all V_{DD} values is 0,3% /°C)

PARAMETER			TEST CONDITIONS			VALUES						UNIT
				V_I (V)	V_{DD} (V)	T_{LOW}*		25°C			T_{HIGH}*	
						min.	max.	min.	typ.	max.	min.	max.	
I_L	Quiescent device current (All switches ON or all switches OFF)	G, H types		0/ 5	5		0.25		0.01	0.25		7.5	μA
				0/10	10		0.5		0.01	0.5		15	μA
				0/15	15		1		0.01	1		30	μA
				0/20	20		5		0.02	5		150	μA
		E, F types		0/ 5	5		1		0.01	1		7.5	μA
				0/10	10		2		0.01	2		15	μA
				0/15	15		4		0.01	4		30	μA

Signal inputs (V_{is}) and Outputs (V_{os})

PARAMETER			TEST CONDITIONS	V_{DD} (V)	T_{LOW}* min.	T_{LOW}* max.	25°C min.	25°C typ.	25°C max.	T_{HIGH}* min.	T_{HIGH}* max.	UNIT
R_{ON}	On resistance	G, H types	$V_C = VDD$ $R_L = 10\ k\Omega$ return to $\frac{V_{DD}-V_{SS}}{2}$ $V_{is} = V_{SS}$ to V_{DD}	5		800		470	1050		1300	Ω
				10		310		180	400		550	Ω
				15		200		125	240		320	Ω
		E, F types		5		850		470	1050		1200	Ω
				10		330		180	400		500	Ω
				15		210		125	240		300	Ω
Δ_{ON}	Resistance Between Any 2 switches, ΔR_{ON}		$R_L = 10k\Omega$, $V_C = V_{DD}$	5				15				Ω
				10				10				Ω
				15				5				Ω
TDH	Total Harmonic Distorsion		$V_C=V_{DD}=5V$, $V_{SS}=-5V$, V_{is} (p–p)=5V (Sine wave centered in 0V) $R_L = 10\ k\Omega$ $f_{is} = 1$ kHz sine wave					0.4				%
-3dB	Cutoff Frequency (switch on)		$V_C=V_{DD}=5V$, $V_{SS}=-5V$, V_{is} (p–p)=5V (Sine wave centered on 0V) $R_L = 1\ k\Omega$					40				MHz
-50dB	Fedthrough Frequency (switch off)		$V_C=V_{DD}=5V$, V_{is} (p–p)=5V (Sine wave centered on 0V) $R_L = 1\ k\Omega$					1				MHz
-50dB	Crosstalk Frequency		$V_C(A) = V_{DD} = +5V$ $V_C(B) = V_{SS} = -5V$ $V_{is}(A) = 5Vp\text{-}p$, 50Ω source $R_L = 1\ k\Omega$					8				MHz
t_{pd}	Propagation delay (Signal Input to Signal output)		$R_L = 200\ k\Omega$ $V_C=V_{DD}$, V_{SS} = GND, C_L=50 pF, $V_{is} = 10V$ (Square wave centred on 5V) $t_r = t_r = 20$ ns		5			20	40			ns
					10			10	20			ns
					15			7	15			ns
C_{is}	Input capacitance		$V_{DD} = +5V$ $V_C=V_{SS} = -5V$					8				pF
C_{os}	Output capacitance							8				pF
C_{ios}	Feedthrough							0.5				pF

PARAMETER		TEST CONDITIONS	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
Input/Output Leakage current switch OFF	G, H types	V_C=0V V_{is}= 18V; V_{os}= 0V V_{is} = 0V; V_{os}= 18V	18		±0.1		$\pm 10^{-3}$	±0.1		±1	µA
	E, F types	V_C=0V V_{is}= 15V; V_{os}= 0V V_{is} = 0V; V_{os}= 15V	15		±0.3		$\pm 10^{-3}$	±0.3		±1	µA
Control (V_C)											
V_{ILC} Control input Low voltage		$\|I_{is}\| < 10$ µA $V_{is} = V_{SS}$, $V_{os} = V_{DD}$ and $V_{is} = V_{DD}$, $V_{os} = V_{SS}$	5		1			1		1	V
			10		2			2		2	V
			15		2			2		2	V
V_{IHC} Control input High voltage			5	3.5		3.5			3.5		V
			10	7		7			7		V
			15	11		11			11		V
I_{IH}, I_{IL} Input leakage current	G, H types	$V_{is} \leq V_{DD}$ $V_{DD} - V_{SS} = 18$ V	18		±0.1		$\pm 10^{-5}$	±0.1		±1	µA
	E, F types	$V_{DD} - V_{SS} = 15$ V $V_{CC} \leq V_{DD} - V_{SS}$	15		±0.3		$\pm 10^{-5}$	±0.3		±1	µA
Crosstalk (control input to signal output)		$V_C = 10$ V (Sq. wave) t_r, t_f = 20 ns R_L = 10 kΩ	10				50				mW
Turn-On propagation delay		$V_{IN} = V_{DD}$, t_r, t_f = 20 ns; C_L = 50 pF, R_L = 1 kΩ	5				35	70			ns
			10				20	40			ns
			15				15	30			ns
Control input Repetition rate		V_{is} =V_{DD}, V_{SS}=GND R_L = 1 kΩ to gnd C_L = 50 pf V_C = 10 V (Square wave centered on 5 V) t_r, t_f = 20 ns $V_{os} = {}^1/_2\, V_{os}$ O 1 KHZ	5				6				MHz
			10				9				MHz
			15				9.5				MHz
C_I Input capacitance		Any input					5	7.5			pF

* $T_{LOW} = -55$°C for G, H devices; -40°C for E, F devices.

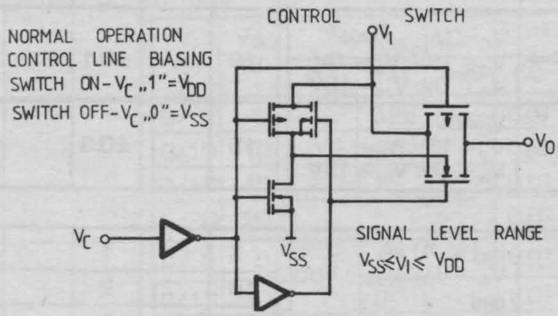
* $T_{HIGH} = +125$°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

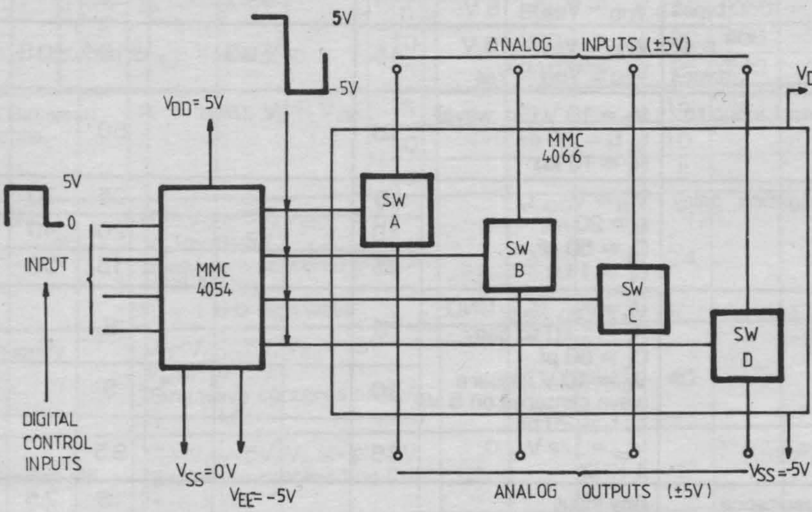
SCHEMATIC DIAGRAM

1 of 4 identical switches and its associated control circuitry



TYPICAL APPLICATIONS

Bidirectional signal transmission via digital control logic



ANALOG MULTIPLEXERS/DEMULTIPLEXERS: MMC 4067: SINGLE 16-CHANNEL MMC 4097: DIFFERENTIAL 8-CHANNEL

GENERAL DESCRIPTION

The MMC 4067, MMC 4097 are monolithic integrated circuits, available in 24-lead dual-in-line plastic package.
The MMC 4067, MMC 4097 analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance, low OFF leakage current, and internal address decoding. In addition, the ON resistance is relatively constant over the full input-signal range.
The MMC 4067 is a 16-channel multiplexer with four binary control inputs A, B, C, D, and an inhibit input, arranged so that any combination of the inputs selects one switch.

The MMC 4097 is a differential 8-channel multiplexer having three binary control inputs A, B, C, and an inhibit input. The inputs permit selection of one of eight pairs of switches. A logic „1" present at the inhibit input turns all channels off.

FEATURES

- Low on resistance: 125Ω (typ.) over 15 V_{p-p} signal-input range for V_{DD}-V_{SS} = 15 V
- High off resistance: channel leakage of +/−10 pA (typ.) for V_{DD}-V_{SS} = 15 V
- Matched switch characteristics: Δ R_{on} = 5Ω (typ). for V_{DD}-V_{SS} = 15 V
- Very low quiescent power dissipation under all digital-control input and supply conditions: 0.2. μW (typ.) for V_{DD}-V_{SS} = 10 V
- Binary address decoding on chip

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

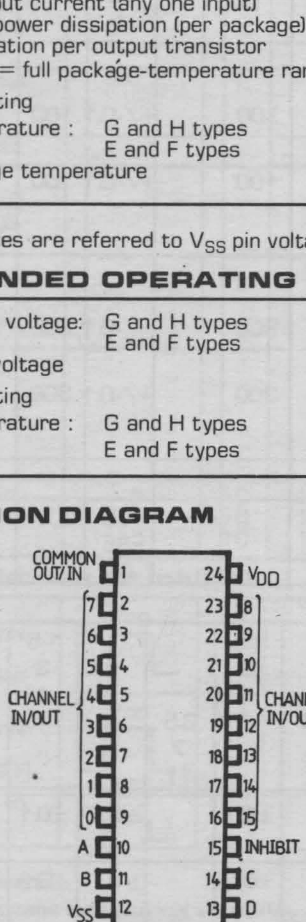
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

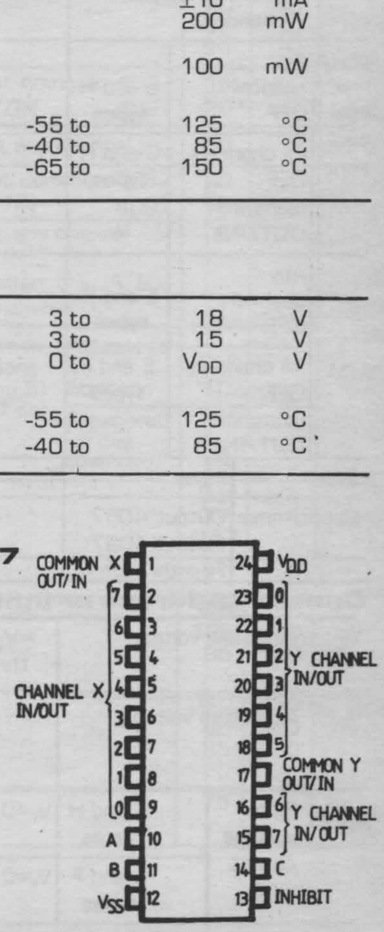
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM

MMC 4067



MMC 4097



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	T_{LOW}(●) min.	T_{LOW}(●) max.	25°C min.	25°C typ	25°C max.	T_{HIGH}(●) min.	T_{HIGH}(●) max.	
I_L	Quiescent device current	G and H types				5 10 15 20		5 10 20 100		0.04 0.04 0.04 0.08	5 10 20 100		150 300 600 3000	µA
		E and F types				5 10 15		20 40 80		0.04 0.04 0.04	20 40 80		150 300 600	µA
Switch														
ON	Resistance	G and H types	$0 \leq V_I \leq V_{DD}$	0	0	5 10 15		800 310 200		470 180 125	1050 400 240		1300 580 320	Ω
		E and F types	$0 \leq V_I \leq V_{DD}$	0	0	5 10 15		850 330 210		470 180 125	1050 400 240		1200 520 300	Ω
ΔON	Resistance (Between any 2 channels)			0	0	5 10 15				10 10 5				Ω
OFF(●) leakage current	Any channel OFF	G and H types		0	0	18		100		+/-0.1	100		1000	nA
	All channels OFF (common OUT/IN)	G and H types		0	0	18		100		+/-0.1	100		1000	nA
	Any channel OFF	E and F types		0	0	15		300		+/-0.1	300		1000	nA
	All channels OFF (common OUT/IN)	E and F types		0	0	15		300		+/-0.1	300		1000	nA
C	Input									5				pF
Capacitance	Output 4067 Output 4097 Feedthrough				−5	5				55 35 0.2				pF
Control (Address or Inhibit)														
V_{IL}	Input low voltage		$=V_{DD}$ thru 1 kΩ	$V_{EE}=V_{SS}$ $R_L = 1K$ to V_{SS}		5 10 15		1.5 3 4			1.5 3 4		1.5 3 4	V
V_{IH}	Input high voltage			$I_{IS} < 2\mu A$ (on all OFF channels)		5 10 15	3.5 7 11		3.5 7 11			3.5 7 11		V
I_{IH}, I_{IL}	Input leakage curent	G and H types	$V_I=0/18$			18		±0.1		$\pm 10^{-3}$	±0.1		±1	µA
		E and F types	$V_I=0/15$			15		±0.3		$\pm 10^{-3}$	±0.3		±1	µA

PARAMETER	TEST CONDITIONS				VALUES							UNIT
	V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
CI Input capacitance	Any address or inhibit input							5	7.5			pF

(●) Determined by minimum feasible leakage measurement for automatic testing

✲ T_{LOW} = −55°C for G and H types; −40°C for E and F types

T_{high} = +125°C for G and H types; +85°C for E and F types

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C, C_L = 50 pF, all input square wave rise and fall times = 20 ns)

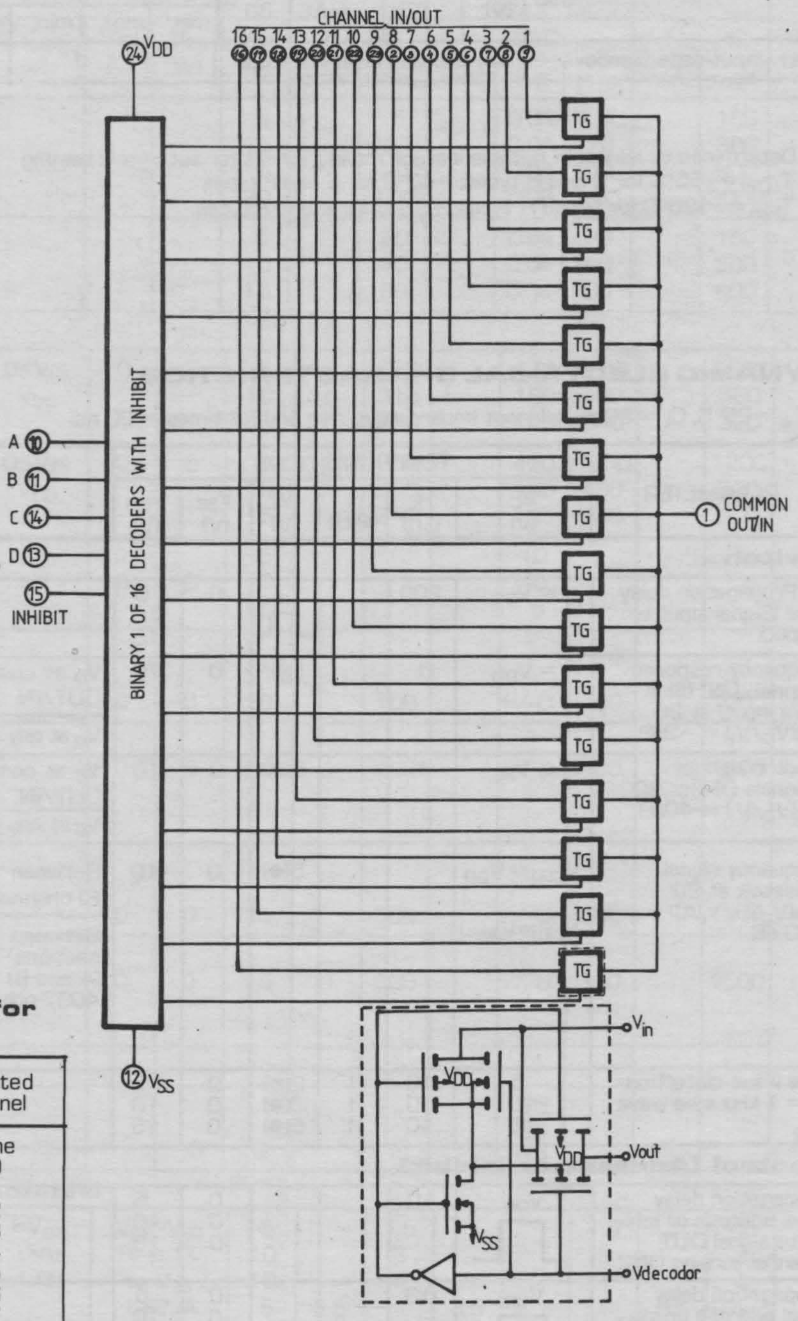
PARAMETER	TEST CONDITIONS							VALUES		UNIT
	V_C (V)	R_L (kΩ)	f_i (kHz)	V_i (V)	V_{SS} (V)	V_{DD} (V)		TYP.	MAX.	
Switch										
t_{pd} Propagation delay time (Signal input to output)	$= V_{DD}$	200		V_{DD}	0	5 10 15		30 15 11	60 30 20	ns
Frequency response channel „ON" (Sine wave input) at 20 Log(V_O/V_i) = −3dB	$= V_{DD}$	1		5(●)	0	10	V_O at common OUT/IN 4067 4097	14 20		MHz
							V_O at any channel	60		MHz
Feedthrough (all channels OFF) at 20 Log(V_O/V_i) = −40dB	$= V_{SS}$	1		5(●)	0	10	V_O at common OUT/IN 4067 4097	20 12		MHz
							V_O at any channel	8		
Frequency signal crosstalk at 20 Log($V_O(B)/V_i(A)$) = −40 dB	$V_{C(A)} = V_{DD}$ $V_{C(B)} = V_{SS}$	1		5(●)	0	10	Between any (A and B) channels	1		
							Between sections (A and B) 4097 only — Measured on common	10		MHz
							Between sections (A and B) 4097 only — Measured on any channel	18		
Sine wave distortion f_{is} = 1 kHz sine wave	5 10 15	10 10 10	1 1 1	2(●) 3(●) 5(●)	0 0 0	5 10 15		0.3 0.2 0.12		%
Control (Address or inhibit)										
Propagation delay time: address or inhibit to signal OUT (channel turning ON)	V_{DD}	10			0 0 0	5 10 15		325 135 95	650 270 190	ns
Propagation delay time: address or inhibit to signal OUT (channel turning OFF)	V_{DD}	0.3			0 0 0	5 10 15		220 90 65	440 180 130	ns
Address or inhibit to signal crosstalk	V_{DD}	10✲			0	10		75		mV peak

✲ Both ends of channel

(●) peak to peak voltage symmetrical about $(V_{DD}-V_{SS})/2$

LOGIC DIAGRAM

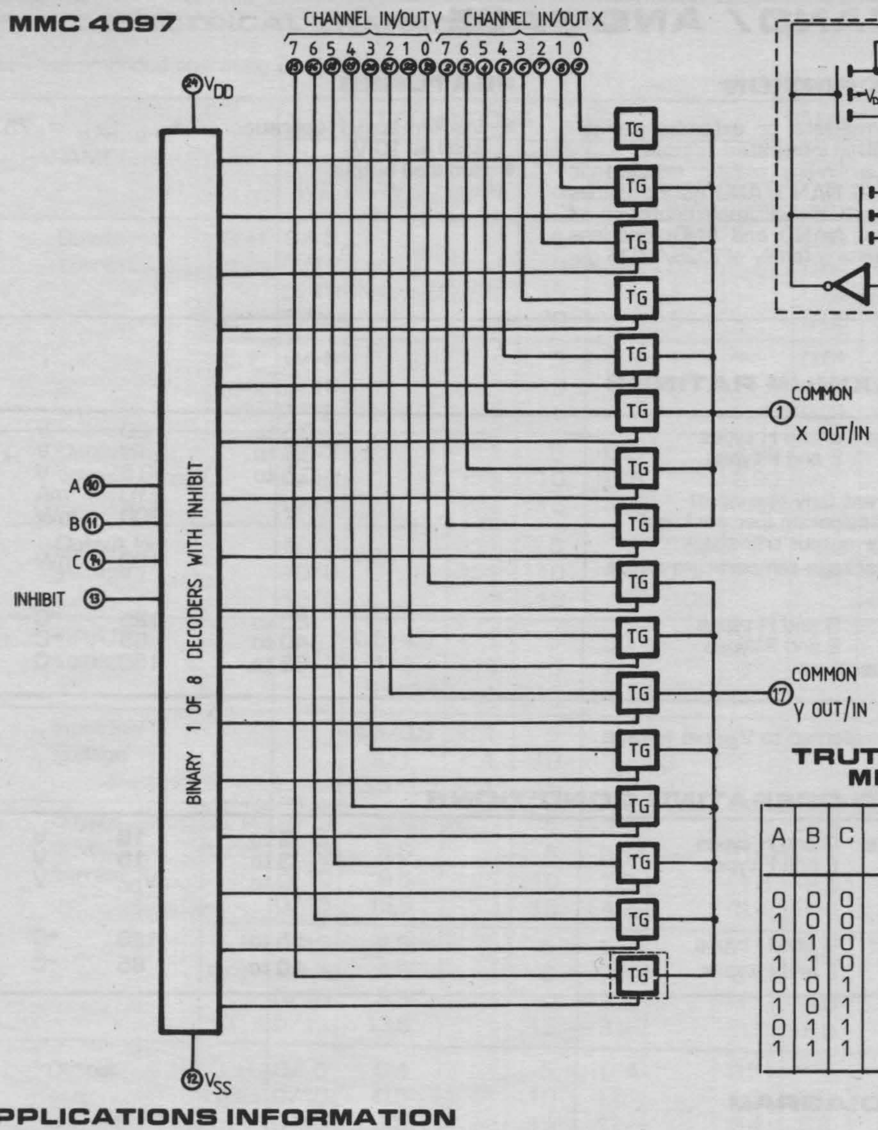
MMC 4067

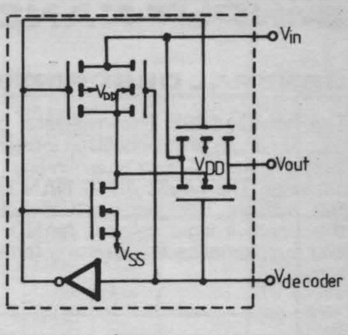


TRUTH TABLE for MMC 4067

A	B	C	D	Inh	Selected channel
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

MMC 4097





TRUTH TABLE for MMC 4097

A	B	C	Inh	Selected channel
0	0	0	0	0X, 0Y
1	0	0	0	1X, 1Y
0	1	0	0	2X, 2Y
1	1	0	0	3X, 3Y
0	0	1	0	4X, 4Y
1	0	1	0	5X, 5Y
0	1	1	0	6X, 6Y
1	1	1	0	7X, 7Y

APPLICATIONS INFORMATION

In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the MMC 4067 or MMC 4097.

When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned on or off by an address input, there is a momentary conductive path from the channel to V_{SS}, which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning on a channel will similarly dump some charge to V_{SS}. The amount of charge dumped is mostly a function of the signal level above V_{SS}. Typically, at $V_{DD}-V_{SS}$ = 10V, a 100 pF capacitor connected to the input or output of the channel will lose3-4% of its voltage at the moment the channel turns on or off. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than1-2 μs. When the inhibit signal turns a channel off, there is no charge dumping to V_{SS}. Rather, there is a slight rise in the channel voltage level (65 mV typ.) due to capacitive coupling from inhibit input to channel input or output. Address inputs also couple some voltage steps onto the channel signal levels.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt

8-INPUT NAND/ AND GATE

GENERAL DESCRIPTION

The MMC 4068 (intermediate or extended temperature range) are monolithic integrated ciorcuit, available in 14-lead dual -in-line plastic or ceramic package. The MMC 4068 NAND/AND gate provides the system designer with direct implementation of the positive-logic 8-input NAND and AND functions and supplements the existing family of COS/MOS gates.

FEATURES

- Medium-speed operation — t_{PHL}, t_{PLH} = 75 ns (typ.) at 10 V
- Buffered output

ABSOLUTE MAXIMUM RATINGS

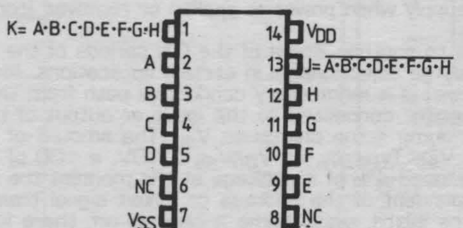
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
		E, F types	0/ 5			5		1		0.01	1		7.5	
			0/10			10		2		0.01	2		15	
			0/15			15		4		0.01	4		30	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V

2 V min. with V_{DD} = 10 V

2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kohm, typical temperature coefficient for all $V_{DD} = 0.3\%/°C$, all input rise and fall times = 20 ns).

PARAMETER		TEST CONDITIONS		VALUES			UNIT
			V_{DD} (V)	min.	typ.	max.	
t_{PHL}, t_{PLH}	Propagation delay time		5		150	300	ns
			10		75	150	
			15		55	110	
t_{TLH}, t_{THL}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	

HEX INVERTER

GENERAL DESCRIPTION

The MMC 4069 is a monolithic integrated circuit processed in standard Al-gate CMOS technology. The MMC 4069 consists of six CMOS inverter circuits. This device is intended for all general-purpose inverter applications where the medium-power TTL-drive and logic-level-conversion capabilities of circuits such as MMC 4049 Hex Inverter/Buffer are not required.

FEATURES

- Medium-speed operation
  t_{PHL}, t_{PLH} = 30 ns (typ.) at 10 V
- Quiescent current specified to 20 V
- 5 V, 10 V, 15 V parametric ratings

ABSOLUTE MAXIMUM RATINGS

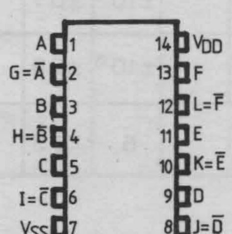
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

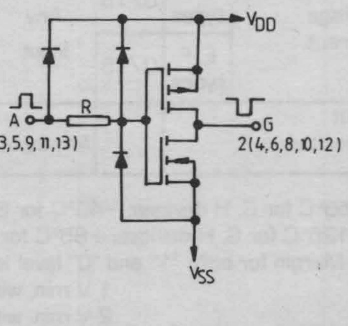
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



SCHEMATIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T_{LOW}^* min.	T_{LOW}^* max.	25°C min.	25°C typ	25°C max.	T_{HIGH}^* min.	T_{HIGH}^* max.	
I_L	Quiescent current	G, H types	0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
		E, F types	0/ 5			5		1		0.01	1		7.5	
			0/10			10		2		0.01	2		15	
			0/15			15		4		0.01	4		30	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	4		4			4		V
				1/9	< 1	10	8		8			8		
				1.5/13.5	< 1	15	12.5		12.5			12.5		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1			1		1	V
				9/1	< 1	10		2			2		2	
				13.5/1.5	< 1	15		2.5			2.5		2.5	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15	Any input		15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200kohm, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall times = 20 ns).

PARAMETER		TEST CONDITIONS	VALUES			UNIT
		V_{DD} (V)	min.	typ.	max.	
t_{PLH}, t_{PHL}	Propagation delay time	5		55	110	ns
		10		30	60	
		15		25	50	
t_{TLH}, t_{THL}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	

QUAD EXCLUSIVE-OR GATE 4070
QUAD EXCLUSIVE-NOR GATE 4077

GENERAL DESCRIPTION

The MMC 4070/4077 are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package.
The MMC 4070 contains four independent exclusive-OR gates.
The MMC 4077 contains four independent exclusive-NOR gates.
The MMC 4070 and MMC 4077 provide the system designer with a means for direct implementation of exclusive-OR and exclusive-NOR function, respectively.

FEATURES

- Medium-speed operation $t_{PHL} = t_{PLH} = 65$ ns (TYP.) at $V_{DD} = 10$ V, $C_L = 50$ pF
- 100% tested for quiescent current

APPLICATIONS

- Logical comparators
- Adders/substractors
- Parity generators and checkers

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

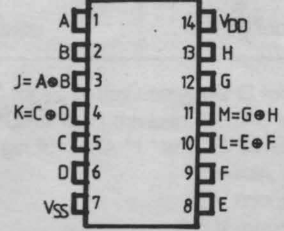
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

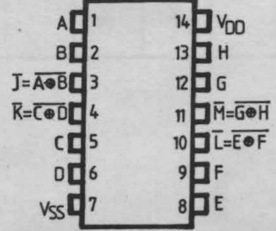
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM

MMC 4070



MMC 4077



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

Parameter			Test conditions V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	Unit
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		mA
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15	Any input		15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

PARAMETER		TEST CONDITIONS	VALUES			UNIT
		V_{CC}(V)	MIN.	TYP.	MAX.	
t_{PHL}, t_{PLH}	Propagation delay time	5 10 15		140 65 50	280 130 100	ns
t_{THL}, t_{TLH}	Transition time	5 10 15		100 50 40	200 100 80	ns

TRUTH TABLE

(1 of 4 gates)

for 4070

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

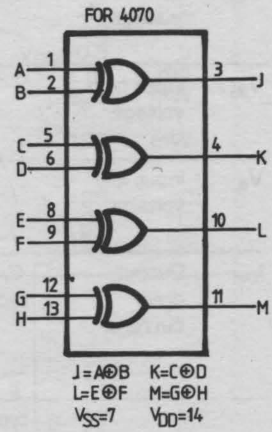
Where 1 = High level
0 = Low level
$J = A \oplus B$

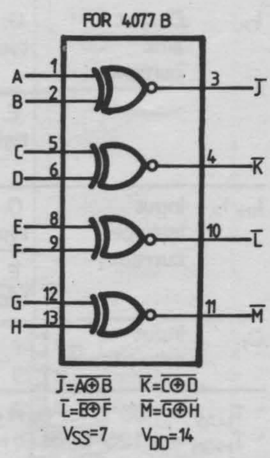
for 4077

A	B	$\overline{J}$
0	0	1
1	0	0
0	1	0
1	1	1

Where 1 = High level
0 = Low level
$\overline{J} = \overline{A \oplus B}$

FUNCTIONAL DIAGRAM





OR Gates: QUAD 2 INPUT MMC 4071 DUAL 4 INPUT MMC 4072 TRIPLE 3 INPUT MMC 4075

GENERAL DESCRIPTION

These OR gates are monolithic complementary MOS (CMOS) integrated circuits. The N and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.
The MMC 4071 MMC 4072 and MMC 4075E/F/G/H/OR gates provide the system designer with direct implementation of the OR function.
All inputs and outputs are buffered.

The MMC 4071 MMC 4072 and MMC 4075 E/F/G/H types are supplied in 14-lead hermetic dual-in-line ceramic or plastic packages.

FEATURES

- Medium-Speed Operation-t_{PLH}, t_{PLH} = 60 ns (typ.) at V_{DD} = 10 V
- 100% tested for quiescent current

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

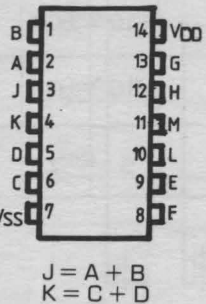
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

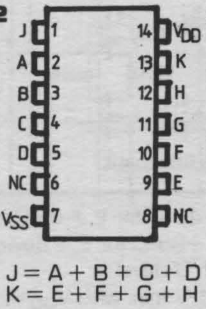
CONNECTION DIAGRAM

MMC 4071



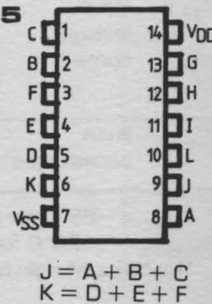
J = A + B
K = C + D
L = E + F
M = G + H

MMC 4072



J = A + B + C + D
K = E + F + G + H

MMC 4075



J = A + B + C
K = D + E + F
L = G + H + I

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
		E, F types	0/ 5			5		1		0.01	1		7.5	
			0/10			10		2		0.01	2		15	
			0/15			15		4		0.01	4		30	
V_{OH}	Output high voltage		0/ 5		<1	5	4.95		4.95			4.95		V
			0/10		<1	10	9.95		9.95			9.95		
			0/15		<1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		<1	5		0.05			0.05		0.05	V
			10/0		<1	10		0.05			0.05		0.05	
			15/0		<1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	<1	5	3.5		3.5			3.5		V
				1/9	<1	10	7		7			7		
				1.5/13.5	<1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	<1	5		1.5			1.5		1.5	V
				9/1	<1	10		3			3		3	
				13.5/1.5	<1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15	Any input		15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V

2 V min. with $V_{DD} = 10$ V

2.5 V min. with $V_{DD} = 15$ V

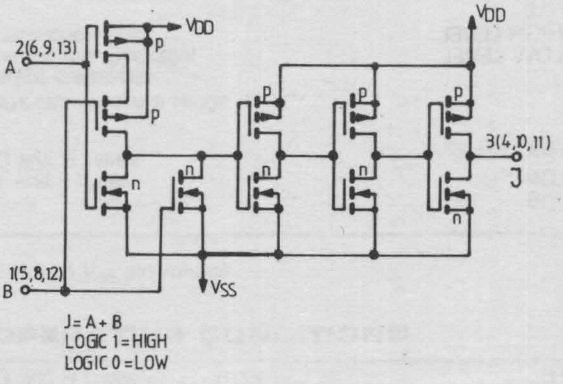
DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$kohm, typical temperature coefficient for all $V_{DD} = 0.3\%/°C$ values, all input rise and fall times = 20 ns).

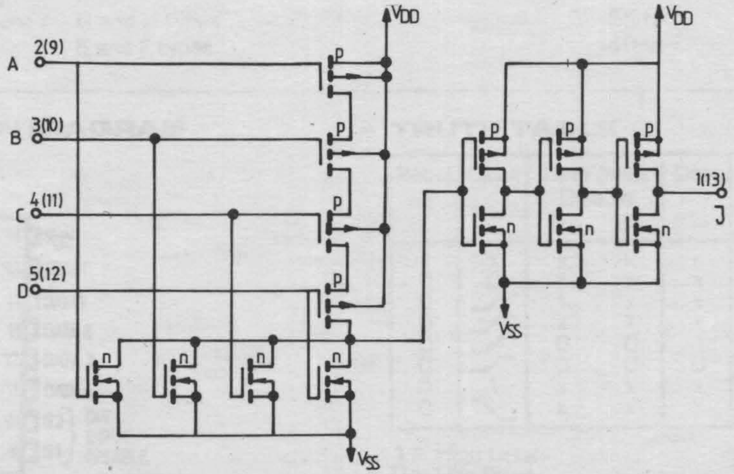
PARAMETER		TEST CONDITIONS	VALUES			UNIT
		V_{DD} (V)	min.	typ.	max.	
t_{PHL}	Propagation delay time	5		125	250	ns
		10		60	120	
		15		45	90	
t_{PLH}	Propagation delay time	5		175	350	ns
		10		70	140	
		15		50	110	
t_{THL} t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	

SCHEMATIC DIAGRAM

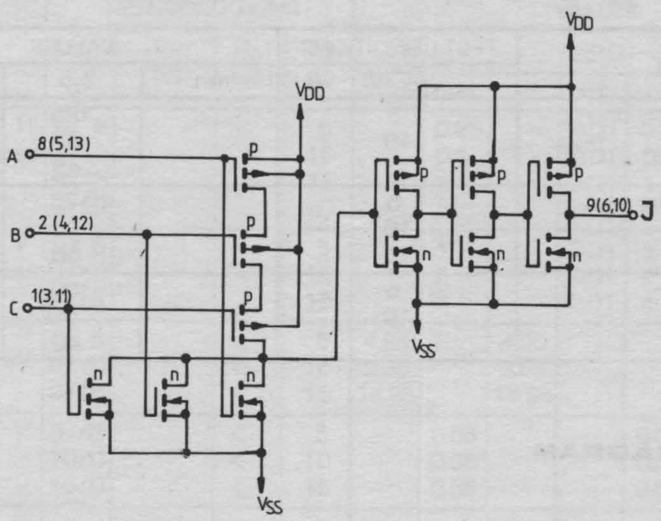
MMC 4071



MMC 4072



MMC 4075



1 = HIGH LEVEL
0 = LOW LEVEL

4BIT D-TYPE REGISTERS

GENERAL DESCRIPTION

The MMC 4076 (intermediate or extended temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package.

The MMC 4076 types are four-bit registers consisting of D-type flip-flops that feature three-state outputs. Data Disable inputs are provided to control the entry of data into the flip-flops. When both Data Disable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Output Disble inputs are also provided. When the Output Disable inputs are both low, the normal logic states of the four outputs are available to the load. The outputs are disabled independently of the clock by a high logic level at either Output Disable input, and present a high impedance.

FEATURES

- Three-state outputs
- Input disabled without gating the clock
- Gated output control lines for enabling or disabling the outputs.

ABSOLUTE MAXIMUM RATINGS

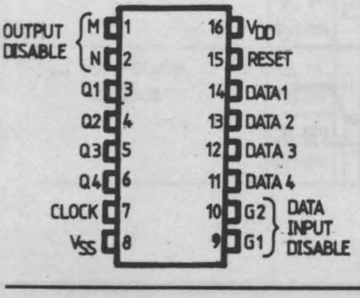
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



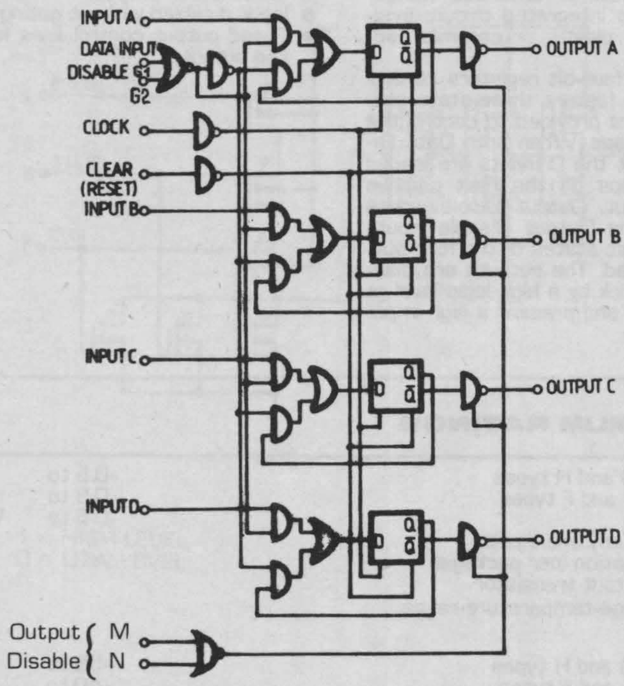
TRUTH TABLE

Reset	Clock	Data Input Disable G_1	Data Input Disable G_2	Data D	Next State Output Q	
1	x	x	x	x	0	
0	0	x	x	x	Q	NC
0	↑	1	x	x	Q	NC
0	↑	x	1	x	Q	NC
0	↑	0	0	1	1	
0	↑	0	0	0	0	
0	1	x	x	x	Q	NC
0	↓	x	x	x	Q	NC

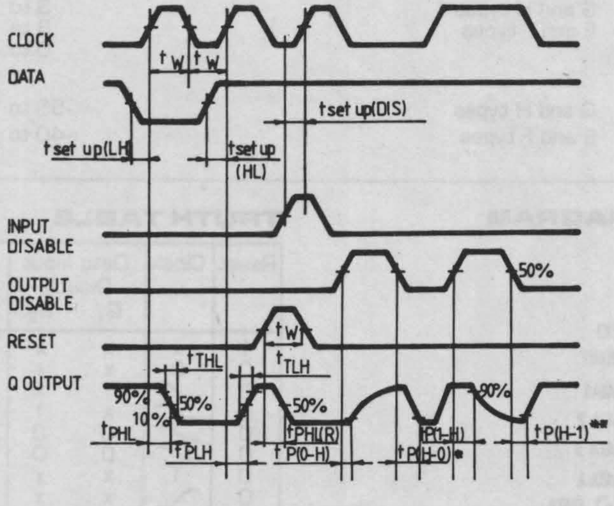
1 = High Level
0 = Low Level

X = Don't Care
NC = No Change

LOGIC DIAGRAM



WAVEFORMS



* Output tied to V_{DD} trough 1 kΩ

** Output tied to V_{SS} trough 1 kΩ

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
							min.	max.	min.	typ	max.	min.	max.	
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	μA
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		
			0/10		< 1	10	9.95		9.95			9.95		V
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	
			10/0		< 1	10		0.05			0.05		0.05	V
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		
				1/9	< 1	10	7		7			7		V
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	
				9/1	< 1	10		3			3		3	V
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		mA
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		mA
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
I_{OH}	3—state output	G, H types	0/18	0/18		18		±0.4		$\pm 10^{-4}$	±0.4		±12	μA
		E, F types	0/15	0/15		15		±1.0		$\pm 10^{-4}$	±1.0		±7.5	

PARAMETER		TEST CONDITIONS				VALUES							UNIT
		V_I (V)	V_O (V)	$\lvert I_O\rvert$ (μA)	V_{DD} (V)	T_{LOW}* Min.	T_{LOW}* Max.	25°C Min.	25°C Typ	25°C Max.	T_{HIGH}* Min.	T_{HIGH}* Max.	
C_I	Input capacitance		Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kohm, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns).

PARAMETER		TEST CONDITIONS	V_{DD} (V)	VALUES min.	typ.	max.	UNIT
t_{PLH}, t_{PHL}	Propagation delay time (clock to Q output)		5 10 15		300 125 90	600 250 180	ns
t_{PHL}(R)	Propagation delay time (Reset)		5 10 15		230 100 75	460 200 150	ns
$t_{P(1-H)}$, $t_{P(0-H)}$	3-state output 1 or 0 to high impedance	$R_L = 1\ k\Omega$	5 10 15		150 75 60	300 150 120	ns
$t_{P(H-1)}$, $t_{P(H-0)}$	3-state high impedance to 1 or 0 output	$R_L = 1\ k\Omega$	5 10 15		150 75 60	300 150 120	ns
t_{TLH}, t_{THL}	Transition time		5 10 15		100 50 40	200 100 80	ns
t_w	Clock pulse width		5 10 15	200 100 80	100 50 40		ns
t_w	Reset pulse width		5 10 15	120 50 40	60 25 20		ns
t_{setup}	Data setup time		5 10 15	200 80 60	100 40 30		ns
t_{setup}	Data input disable setup time		5 10 15	180 100 70	90 50 35		ns
f_{max}	Maximum clock frequency		5 10 15	3 6 8	6 12 16		MHz
t_r, t_f	Clock input rise or fall time		5 10 15	15 5 5			μs

8-INPUT NOR/OR GATE

GENERAL DESCRIPTION

The MMC 4078 (intermediate or extended temperature range) are monolithic integrated circuits available in 14-lead dual-in-line plastic or ceramic package.
The MMC 4078 NOR/OR Gate provides the system designer with direct implementation of the positive-logic-8-input NOR and OR function and supplements the existing family of COS/MOS gates.

FEATURES

- Medium-speed operation t_{PHL}, t_{PLH} = 75 ns (typ.) at V_{DD} = 10 V
- 100% tested for quiescent current

ABSOLUTE MAXIMUM RATINGS

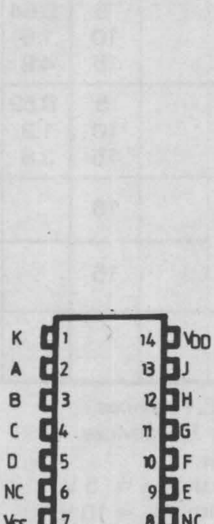
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
		E, F types	0/ 5			5		1		0.01	1		7.5	
			0/10			10		2		0.01	2		15	
			0/15			15		4		0.01	4		30	
V_{OH}	Output high voltage		0/ 5		<1	5	4.95		4.95			4.95		V
			0/10		<1	10	9.95		9.95			9.95		
			0/15		<1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		<1	5		0.05			0.05		0.05	V
			10/0		<1	10		0.05			0.05		0.05	
			15/0		<1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	<1	5	3.5		3.5			3.5		V
				1/9	<1	10	7		7			7		
				1.5/13.5	<1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	<1	5		1.5			1.5		1.5	V
				9/1	<1	10		3			3		3	
				13.5/1.5	<1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V

2 V min. with $V_{DD} = 10$ V

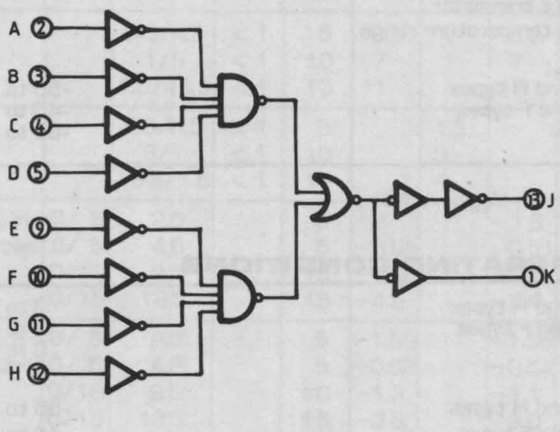
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kohm, typical temperature coefficient for all $V_{DD} = 0.3\%/°C$, all input rise and fall times = 20 ns).

PARAMETER		TEST CONDITIONS	VALUES			UNIT
		V_{DD} (V)	min.	typ.	max.	
t_{PHL}, t_{PLH}	Propagation delay time	5 10 15		150 75 55	300 150 110	ns
t_{TLH}, t_{THL}	Transition time	5 10 15		100 50 40	200 100 80	ns

LOGIC DIAGRAM



CMOS AND GATES:
4081 QUAD 2 - INPUT AND GATE
4082 DUAL 4 - INPUT AND GATE
4073 TRIPLE 3 - INPUT AND GATE

GENERAL DESCRIPTION

The MMC 4081, MMC 4082 and MMC 4073, AND gates provide the system designer with direct implementation of the AND function and supplement the existing family of COS/MOS gates.
The MMC 4081, MMC 4082 and MMC 4073 types are supplied in 14 — lead dual — in — line ceramic or plastic packages.

FEATURES

- Medium speed operation t_{PLH} = 85 ns (TYP); t_{PHL} = 65 ns (TYP) at 10 V
- Quiescent current specified to 20 V

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

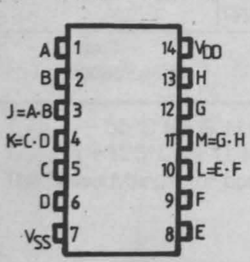
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

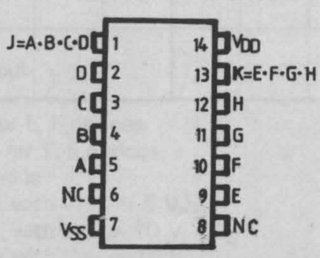
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM

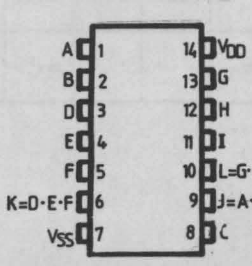
MMC 4081



MMC 4082



MMC 4073



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
							min.	max.	min.	typ	max.	min.	max.	
I_L	Quiescent current	G, H types	0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
		E, F types	0/ 5			5		1		0.01	1		7.5	
			0/10			10		2		0.01	2		15	
			0/15			15		4		0.01	4		30	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V

2 V min. with V_{DD} = 10 V

2.5 V min. with V_{DD} = 15 V

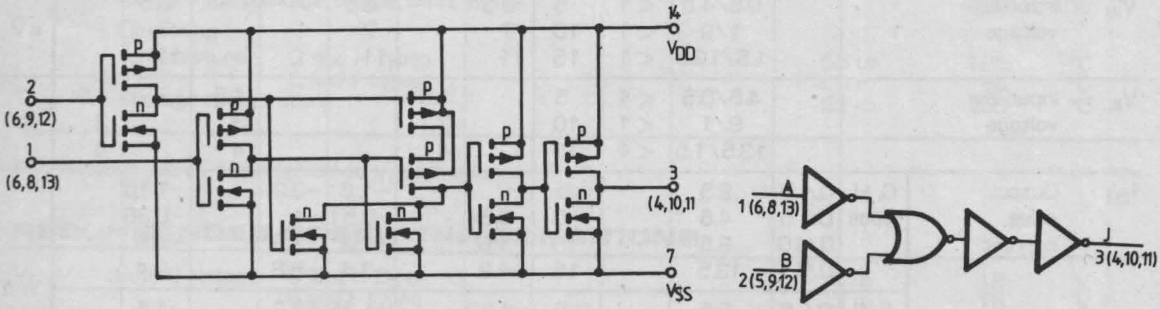
DYNAMIC ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C, C_L = 50 pF, R_L = 200k, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

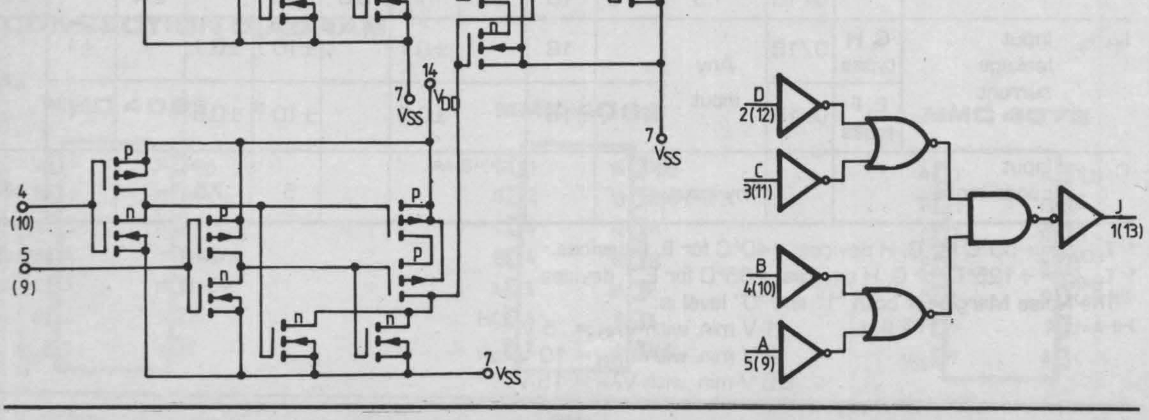
PARAMETER		TEST CONDITIONS	VALUES			UNIT
		V_{DD} (V)	min	typ	max	
t_{PLH}, t_{PHL}	Propagation delay time	5 10 15		125 60 45	250 120 90	ns
t_{THL}, t_{TLH}	Transition time	5 10 15		100 50 40	200 100 80	ns

SCHEMATIC AND LOGIC DIAGRAMS

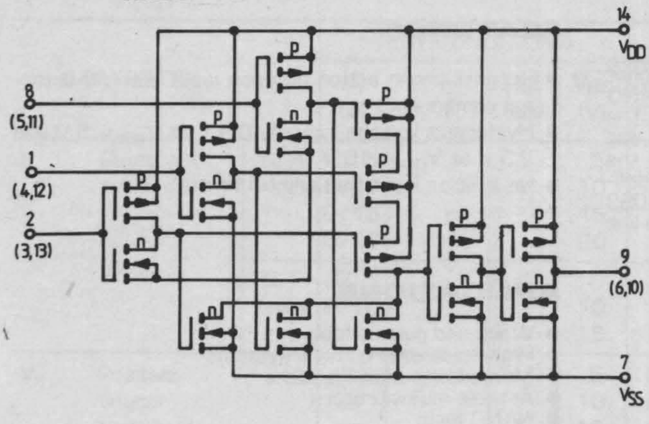
MMC 4081

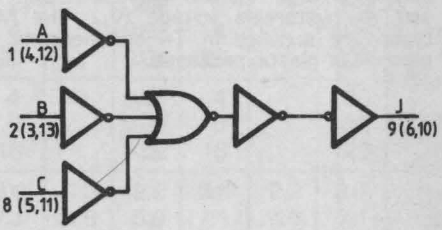


MMC 4082



MMC 4073





QUAD 2-INPUT NAND SCHMITT TRIGGERS

GENERAL DESCRIPTION

The MMC 4093 consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate Switches at different points for positive and negative going signals. The difference between the positive voltage (V_P) and negative voltage (V_N) is defined as hysteresis voltage (V_H). The MMC 4093 types are supplied in 14-lead hermetic dual-in-line ceramic or plastic packages.

FEATURES

- Schmitt-triger action on each input with no external components
- Hysteresis voltage typically 0.9 V at V_{DD} = 5 V and 2.3 V at V_{nn} = 10 V
- No limit on input rise and fall times

APLICATIONS

- Wave and pulse shapers
- High-noise-environment systems
- Monostabile multivibrators
- Astable multivibrators
- NAND logic

ABSOLUTE MAXIMUM RATINGS

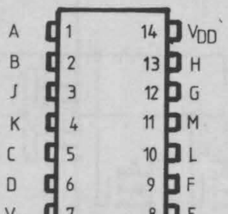
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



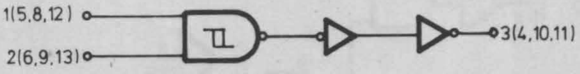
$J = \overline{A \cdot B}$

$K = \overline{C \cdot D}$

$L = \overline{E \cdot F}$

$M = \overline{G \cdot H}$

FUNCTIONAL DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_P	Positive trigger threshold voltage		a			5	2.2	3.6	2.2	2.9	3.6	2.2	3.6	V
			a			10	4.6	7.1	4.6	5.9	7.1	4.6	7.1	
			a			15	6.8	10.8	6.8	8.8	10.8	6.8	10.8	
			b			5	2.6	4	2.6	3.3	4	2.6	4	
			b			10	5.6	8.2	5.6	7	8.2	5.6	8.2	
			b			15	6.3	12.7	6.3	9.4	12.7	6.3	12.7	
V_N	Negative trigger threshold voltage		a			5	0.9	2.8	0.9	1.9	2.8	0.9	2.8	V
			a			10	2.5	5.2	2.5	3.9	5.2	2.5	5.2	
			a			15	4	7.4	4	5.8	7.4	4	7.4	
			b			5	1.4	3.2	1.4	2.3	3.2	1.4	3.2	
			b			10	3.4	6.6	3.4	5.1	6.6	3.4	6.6	
			b			15	4.8	9.6	4.8	7.3	9.6	4.8	9.6	
V_H	Hysteresis voltage		a			5	0.3	1.6	0.3	0.9	1.6	0.3	1.6	V
			a			10	1.2	3.4	1.2	2.3	3.4	1.2	3.4	
			a			15	1.6	5	1.6	3.5	5	1.6	5	
			b			5	0.3	1.6	0.3	0.9	1.6	0.3	1.6	
			b			10	1.2	3.4	1.2	2.3	3.4	1.2	3.4	
			b			15	1.6	5	1.6	3.5	5	1.6	5	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		

a: input on terminals 1, 5, 8, 12 or 2, 6, 9, 13; other inputs to V_{DD}.
b: input on terminals 1 and 2, 5 and 6, 8 and 9, or 12 and 13; other inputs to V_{DD}.

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

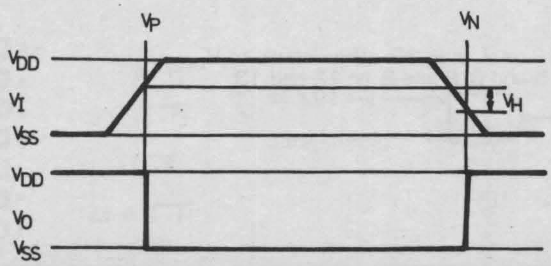
* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.
* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

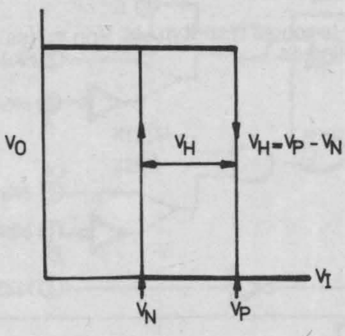
($T_A = 25°C$; input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kohm)

PARAMETER		TEST CONDITIONS V_{DD} (V)	VALUES min.	typ.	max.	UNIT
t_{PHL}, t_{PLH}	Propagation delay time	5		190	300	ns
		10		90	180	
		15		65	90	
t_{THL}, t_{THL}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	

Fig. 1 Hysteresis definition, characteristic and test setup
(a) Definition of V_P, V_N and V_H



(b) Transfer characteristic of 1 of 4 gates



(c) Test setup

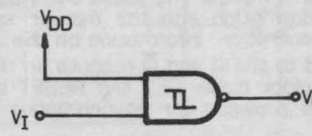
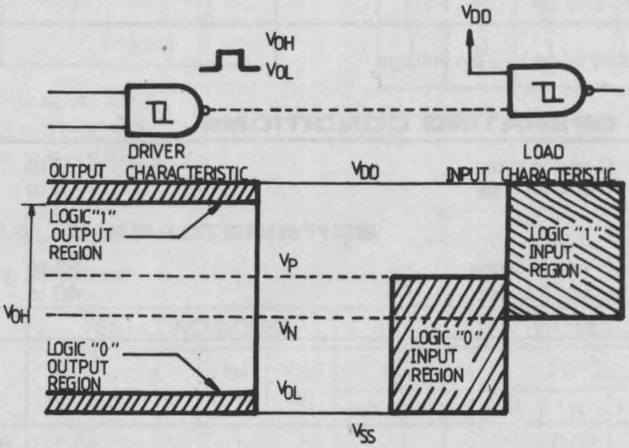


Fig. 2 Input and output characteristics



GATED J-K MASTER-SLAVE FLIP-FLOPS

GENERAL DESCRIPTION

The MMC 4095/4096 (intermediate or extended temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package.
The MMC 4095 and MMC 4096 are J-K Master-Slave Flip-Flops featuring separate AND gating of multiple J and K inputs. The gated J-K inputs control tansfer of information into the master section during clocked operation. Information on the J-K inputs is transferred to the Q and $\overline{Q}$ outputs on the positive edge of the clock pulse. SET and RESET inputs (active high) are provided for asynchronous operation.

FEATURES

- 16 MHz toggle rate (typ.) at $V_{DD} - V_{SS} = 10$ V
- Gated inputs.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_i	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		±10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

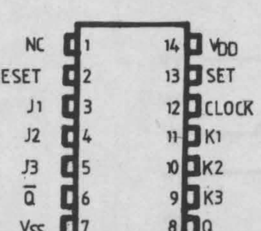
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

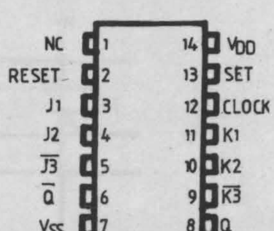
V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_i	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM

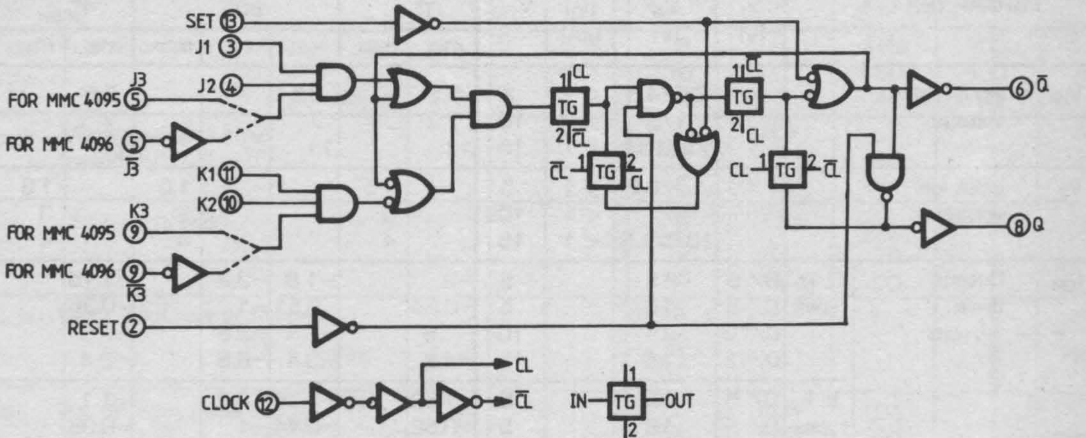
MMC 4095



MMC 4096



LOGIC DIAGRAM



TRUTH TABLES

SYNCHRONOUS OPERATION

(S = O R = O)

Inputs before positive clock transition		Outputs after positive clock transition	
J*	K*	Q	Q
0	0	No change	
0	1	0	1
1	0	1	0
1	1	Toggles	

* For MMC 4095
J = J1·J2·J3
K = K1·K2·K3

For MMC 4096
$J = J1 \cdot J2 \cdot \overline{J3}$
$K = K1 \cdot K2 \cdot \overline{K3}$

ASYNCHRONOUS OPERATION

(J and K — DON'T CARE)

S	R	Q	Q
0	0	No change	
0	1	0	1
1	0	1	0
1	1	0	0

$0 = V_{SS}$, $1 = V_{DD}$

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
							min.	max.	min.	typ	max.	min.	max.	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

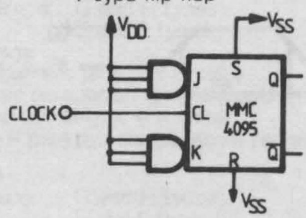
(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} = 0.3%/°C all input rise and fall times = 20 ns).

PARAMETER		TEST CONDITIONS	VALUES			UNIT
		V_{DD} (V)	min.	typ.	max.	
t_{PLH}, t_{PHL}	Propagation delay time	5		250	500	ns
		10		100	200	
		15		75	150	
t_{PLH}, t_{PHL}	Propagation delay time (Set or reset)	5		150	300	ns
		10		75	150	
		15		50	100	

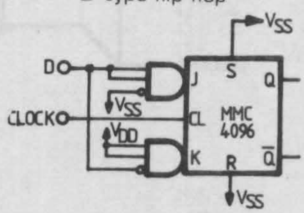
	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES min.	VALUES typ.	VALUES max.	UNIT
t_{THL}, t_{TLH}	Transition time	5 10 15		100 50 40	200 100 80	ns
f_{CL}	Maximum clock input frequency	5 10 15	3.5 8 12	7 16 24		MHz
t_W	Clock pulse width	5 10 15	140 60 40	70 30 20		ns
t_r, t_f	Clock input rise or fall time	5 10 15			15 5 5	µs
t_W	Set or reset pulse width	5 10 15	200 100 50	100 50 25		ns
t_{setup}	Data setup time	5 10 15	400 160 100	200 80 50		ns

TYPICAL APPLICATIONS

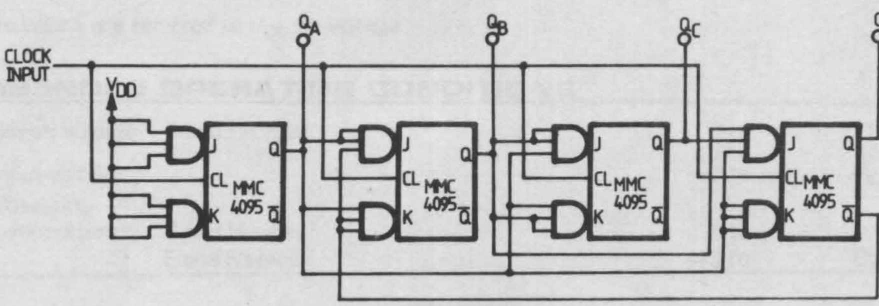
T-type flip-flop

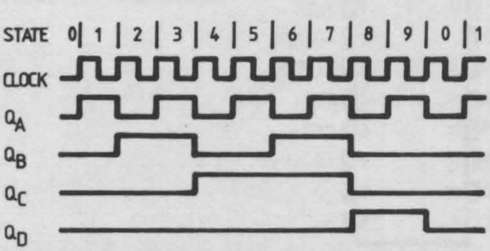


D-type flip-flop



Synchronous binary divide-by-ten counter



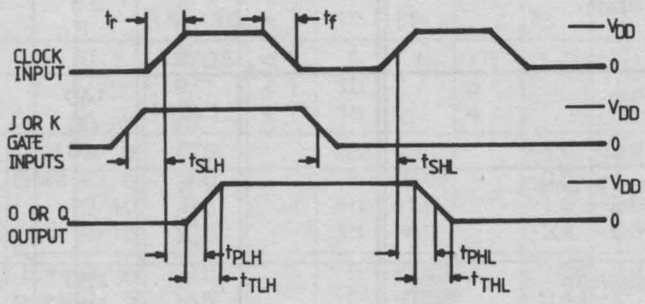


STATE	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

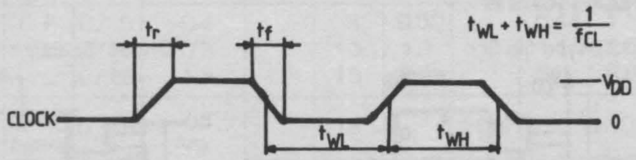
In all MMC 4095 units the Set and Reset are connected to V_{SS}

WAVEFORMS

Propagation delay, transition and setup-time



Clock pulse rise and fall time



DUAL MONOSTABLE MULTIVIBRATOR

GENERAL DESCRIPTION

The MMC 4098 is a monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package. The MMC 4098 dual monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application. An external resistor (R_X) and an external capacitor (C_X) control the timing for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_x and C_x.

Leading-edge-triggering (+TR) and trailing-edge-triggering (−TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to V_{SS}. An unused −TR input should be tied to V_{DD}. A $\overline{RESET}$ (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to V_{DD}. However, if an entire section of the MMC 4098 is not used, its RESET should be tied to V_{SS}. See Table I. In normal operation the circuit triggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-triggerable mode, Q is connected to −TR when leading-edge triggering(+TR) is used or Q is connected to +TR when trailing-edge triggering (−TR) is used. The time period (T) for this multivibrator can be approximated by: $T_X = \frac{1}{2} R_X C_X$ for $C_X \geq 0.01 \mu F$. Values of T vary from unit to unit and as a function of voltage, temperature, and $R_x C_x$. The minimum value of external resistance, R_x, is 5 kΩ. The maximum value of external capacitance, C_x, is 100 μF. The output pulse width has variations of ±2,5% typically over the temperature range of −55°C to 125°C for C_x = 1000 pF and Rx = 100 kΩ.

For power supply variations of ±5%, the output pulse width has variations of ±0,5% tipically, for V_{DD} = 10 V and 15 V and ±1% typically, for V_{DD} = 5 V at C_x = 1000 pF and R_x = 5 kΩ.

FEATURES

- Retriggerable/resettable capability
- Trigger and reset propagation delays independent of R_X,C_X
- Triggering from leading or trailing edge
- Q and $\overline{Q}$ buffered outputs available
- Separate resets
- Wide range of output-pulse widths

ABSOLUTE MAXIMUM RATINGS

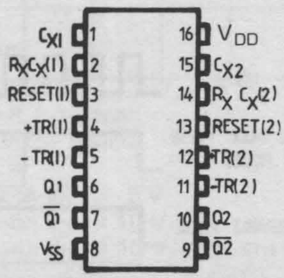
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

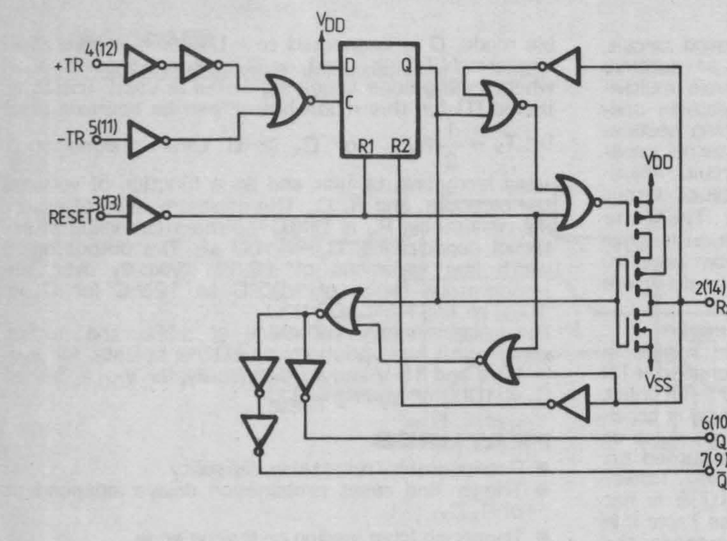
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



LOGIC DIAGRAM



FUNCTIONAL DIAGRAM

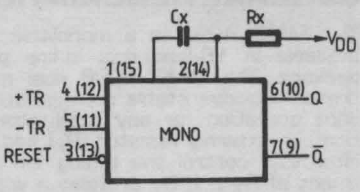
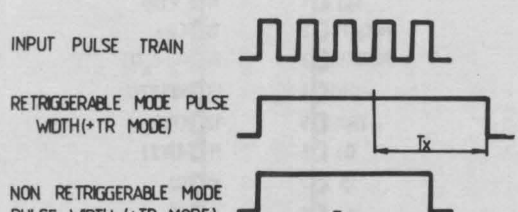


TABLE I

— Functional terminal connections

FUNCTION	TERMINAL CONNECTIONS TO VDD Mono (1)	VDD Mono (2)	TO VSS Mono (1)	VSS Mono (2)	INPUT PULSE TO Mono (1)	Mono (2)	OTHER CON-NECTIONS Mono (1)	Mono (2)
Leading-Edge Trigger/Retriggerable	3,5	11,13			4	12		
Leading-Edge Trigger/Non-retriggerable	3	13			4	12	5,7	11,9
Trailing-Edge Trigger/Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/Non-retriggerable	3	13			5	11	4,6	12,10
Unused Section	5	11	3,4	12,13				

NOTES: 1) A Retriggerable one-shot multivibrator has an output pulse width which is extended one full time period (T_X) after application of the last trigger pulse.
2) A Non-retriggerable one-shot multivibrator has a time period T_X referenced from the application of the first trigger pulse.



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

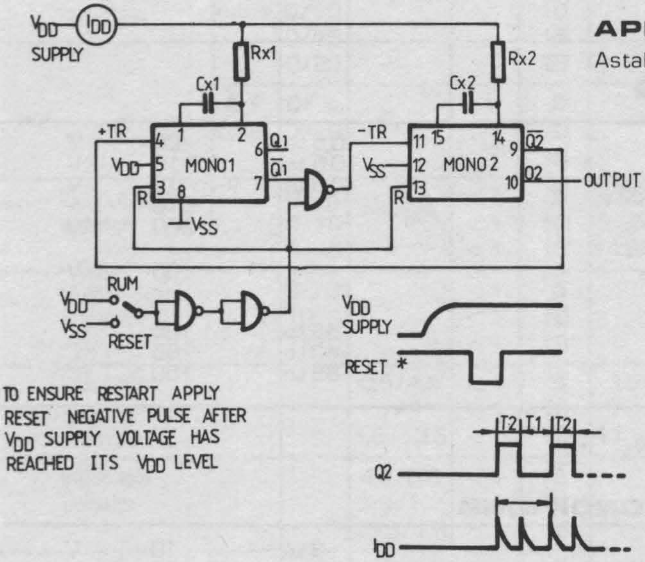
(T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20 ns)

	PARAMETER	TEST CONDITIONS			VALUES			UNIT
		R_X (kΩ)	C_X (pF)	V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH},	Trigger propagation delay	5 to	≥15	5		250	500	
t_{PHL}	time (+TR, −TR to Q, $\overline{Q}$)	10 000		10		125	250	ns
				15		100	200	
t_{WH},	Trigger pulse width	5 to	≥15	5	140	70		
t_{WL}		10 000		10	60	30		ns
				15	40	20		
t_{TLH}	Transition time	5 to	≥15	5		100	200	
		10 000		10		50	100	
				15		40	80	
t_{THL}	Transition time	5 to	15 to	5		100	200	
		10 000	10 000	10		50	100	
				15		40	80	ns
		5 to	0.01 µF	5		150	300	
		10 000	to	10		75	150	
			0.1 µF	15		65	130	
		5 to	0.1 µF	5		250	500	
		10 000	to	10		150	300	
			1 µF	15		80	160	
t_{PLH},	Propagation delay time	5 to		5		225	450	
t_{PHL}	(Reset)	10 000	≥15	10		125	250	ns
				15		75	150	
t_{WR}	Pulse width (Reset)			5	200	100		
			15	10	80	40		
				15	60	30		ns
				5	1 200	600		
		100	1 000	10	600	300		
				15	500	250		
				5	50	25		
			0.1 µF	10	30	15		µs
				15	20	10		
t_r, t_f	(TR) Rise or fall time (Trigger)			5 to 15			100	µs

PARAMETER	TEST CONDITIONS			VALUES			UNIT
	R_X (kΩ)	C_X (pF)	V_{DD} (V)	Min.	Typ.	Max.	
Pulse width match between circuits in same package	10	10 000	5		5	10	%
			10		7.5	15	
			15		7.5	15	

APPLICATIONS

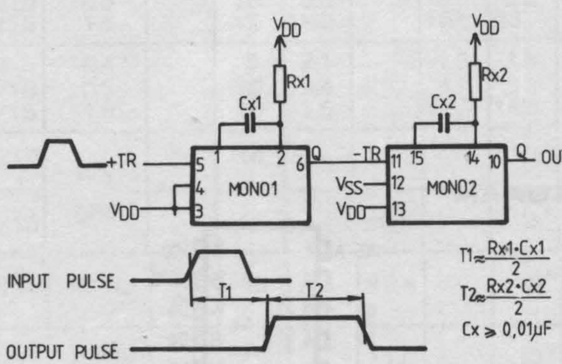
Astable multivibrator with restart after reset capability



R_X	I_{DD} (Avg)	T_X (T1+T2)	V_{DD}
10 kΩ	1 mA / 0.05 mA	3.8 s / 0.5 s	5 V
↓	2.5 mA ↕ 0.5 mA	3.2 s ↕ 0.5 s	10 V
10 MΩ	5 mA / 1 mA	3 s / 0.5 s	15 V

NOTE:
ALL VALUES ARE TYPICAL
C_x RANGE: 0,0001 μF TO 0,1 μF

Pulse delay



HEX NON-INVERTING TRI-STATE BUFFER

GENERAL DESCRIPTION

The MMC 4503 is a hex non-inverting TRI-STATE buffer with high output current sink and source capability. TRI-STATE outputs make it useful in bus oriented applications. Two separate disable inputs are provided. Buffers 1 to 4 are controlled by the disable A input. Buffers 5 and 6 are controlled by the disable B input. A high level on either disable input will cause those gates on its control line to go into a high impedance state.

FEATURES

- Wide supply voltage range 3.0 V_{DC} to 18 V_{DC}
- TRI-STATE outputs
- Symmetrical turn on/turn off delays
- Symmetrical output rise and fall times
- 1 TTL-load output drive capability
- 2 output-disable controls
- 100% tested for quiescent current

ABSOLUTE MAXIMUM RATINGS

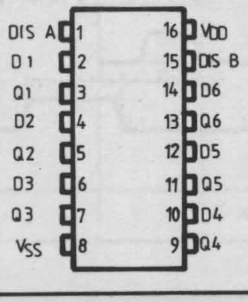
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
							min.	max.	min.	typ	max.	min.	max.	
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	-5.8		-4.8	-6.1		-3		mA
			0/ 5	4.6		5	-1.2		-1.02	-1.9		-0.7		
			0/10	9.5		10	-3.1		-2.6	-3.7		-1.8		
			0/15	13.5		15	-8.2		-6.8	-14.1		-4.8		
		E, F types	0/ 5	2.5		5	-4.8		-4.1	-5.2		-2.9		
			0/ 5	4.6		5	-1		-0.8	-1.6		-0.6		
			0/10	9.5		10	-2.5		-2.2	-3.1		-1.6		
			0/15	13.5		15	-6.8		-5.8	-11.9		-4.2		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	2.6		2.1	2.3		1.3		mA
			0/10	0.5		10	6.5		5.5	2.6		3.8		
			0/15	1.5		15	19.2		16.1	23		11.2		
		E, F types	0/ 5	0.4		5	2.1		1.8	1.9		1.2		
			0/10	0.5		10	5.4		4.7	5.3		3.3		
			0/15	1.5		15	1.6		13.7	19.5		9.7		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
I_{OH}	3—state output	G, H types	0/18	0/18		18		±0.4		$\pm 10^{-4}$	±0.4		±12	μA
		E, F types	0/15	0/15		15		±1.0		$\pm 10^{-4}$	±1.0		±7.5	

PARAMETER		TEST CONDITIONS				VALUES							UNIT
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
						min.	max.	min.	typ	max.	min.	max.	
C_I	Input capacitance		Any input						5	7.5			pF

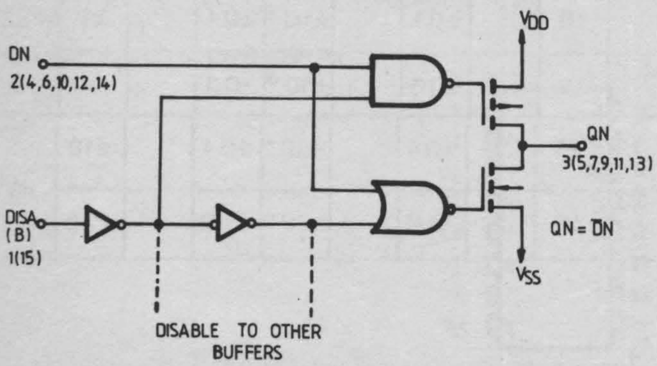
* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 k, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20 ns)

PARAMETER		TEST CONDITIONS V_{DD}(V)	VALUES min.	typ.	max.	UNIT
t_{PLH}, t_{PHL}	Propagation delay time Low-to-High	5		75	150	
		10		35	70	
		15		25	50	
	High-to-Low	5		55	110	ns
		10		25	50	
		15		17	35	
t_{PHZ}, t_{PZH}	3—state propagation delay time	5		70	140	
		10		30	60	
		15		25	50	
t_{PZL}, t_{PLZ}	3—state propagation delay time	5		90	180	ns
		10		40	80	
		15		35	70	
t_{TLH}, t_{THL}	Transition time Low-to-High	5		50	90	
		10		30	45	
		15		25	35	
	High-to-Low	5		35	70	ns
		10		20	40	
		15		13	25	

LOGIC DIAGRAM AND TRUTH TABLE



DN	DISA(B)	QN
0	0	0
1	0	1
X	1	HIGH Z

DUAL 4-BIT LATCH

The MMC 4508 dual 4-bit latch contains two identical 4-bit latches with separate STROBE, RESET and OUTPUT DISABLE controls. With the STROBE line in high state, the data on the "D" inputs appear at the corresponding "Q" outputs provided the DISABLE line is in the low state. Changing the STROBE line to the low state locks the data into the latch. A high on the RESET line forces the outputs to a low level regardless of the state of the STROBE input. The outputs are forced to the high-impedance state for bus line application by a high level on the DISABLE input.
The MMC 4508 E/F/G/H types are supplied in the 24-lead dual-in-line ceramic or plastic packages.

FEATURES

- Two independent 4-bit latches
- Individual master reset for each 4-bit latch
- 3-state outputs with high-impedance state for bus line applications
- Medium-speed operation: $t_{PLH} = t_{PHL} = 70$ ns (typ.) at $V_{DD} = 10$ V and $C_L = 50$ pF

APPLICATIONS

- Buffer storage
- Holding register
- Data storage and multiplexing

ABSOLUTE MAXIMUM RATINGS

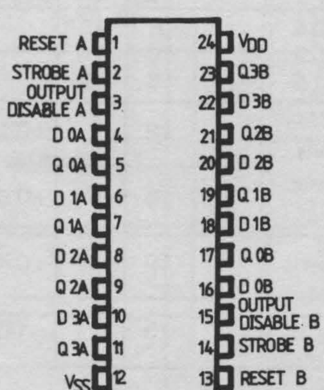
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
I_{OH}	3-state output	G, H types	0/18	0/18		18		±0.4		±10 [illegible]	±0.4		±12	μA
		E, F types	0/15	0/15		15		±1.0		±10 [illegible]	±1.0		±7.5	

PARAMETER	TEST CONDITIONS				VALUES							UNIT
	V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
					min.	max.	min.	typ	max.	min.	max.	
C_I —Input capacitance		Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

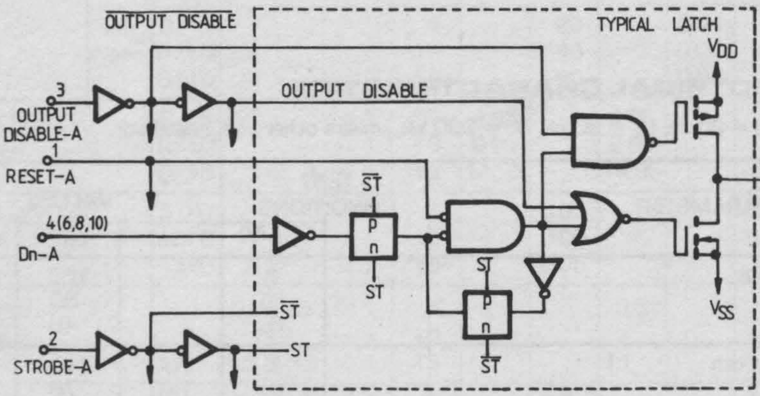
(T_A = 25°C, input t_r, t_f = 20 ns, C_L = 50 pF, R_l = 200 kΩ, unless otherwise specified)

PARAMETER			TEST CONDITIONS V_{DD} (V)	VALUES min.	typ.	max.	UNIT
t_{THL}, t_{TLH}	Transition time		5 10 15		100 50 40	200 100 80	ns
t_W(R)	Reset pulse width		5 10 15	200 140 100	100 70 50		ns
t_W(st)	Strobe pulse width		5 10 15	140 80 70	70 40 35		ns
t_{setup}	Setup time		5 10 15	50 30 20	25 15 10		ns
t_H	Hold time		5 10 15	0 0 0	0 0 0		ns
t_{PHL}, t_{PLH}	Propagation delay times:	Strobe to data out	5 10 15		130 70 50	260 140 100	ns
		Data in to data out	5 10 15		105 60 45	210 120 90	ns
		Reset to data out	5 10 15		90 50 40	180 100 80	ns
t_{PHZ}	3-state propagation delay times: output high to high impedance		5 10 15		90 50 35	180 100 70	ns
t_{PZH}	High impedance to output high		5 10 15		90 50 35	180 100 70	ns
t_{PLZ}	Output low to high impedance		5 10 15		90 50 35	180 100 70	ns

	PARAMETER	TEST CONDITIONS		VALUES			UNIT
			V_{DD} (V)	min.	typ.	max.	
t_{PZL}	High impedance to output low		5 10 15		90 50 35	180 100 70	ns

LOGIC DIAGRAM (A Section)

1 of 4 identifical latches with common output disable, reset and strobe



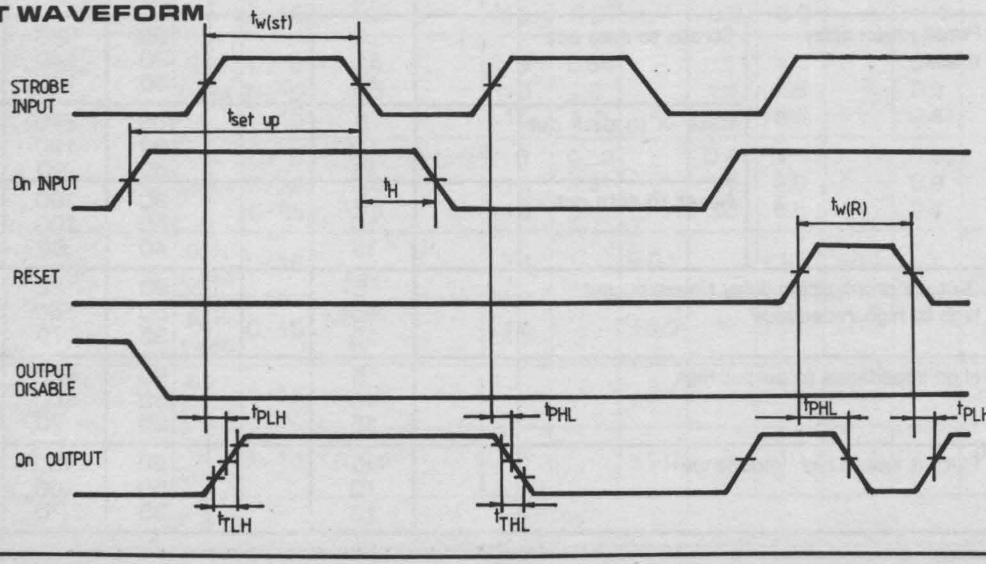
TRUTH TABLE

RESET	DISAB	STROBE	D INPUT	Q INPUT
0	0	1	1	1
0	0	1	0	0
0	0	0	X	Latched
1	0	X	X	0
X	1	X	X	Z

1 = High level
0 = Low level

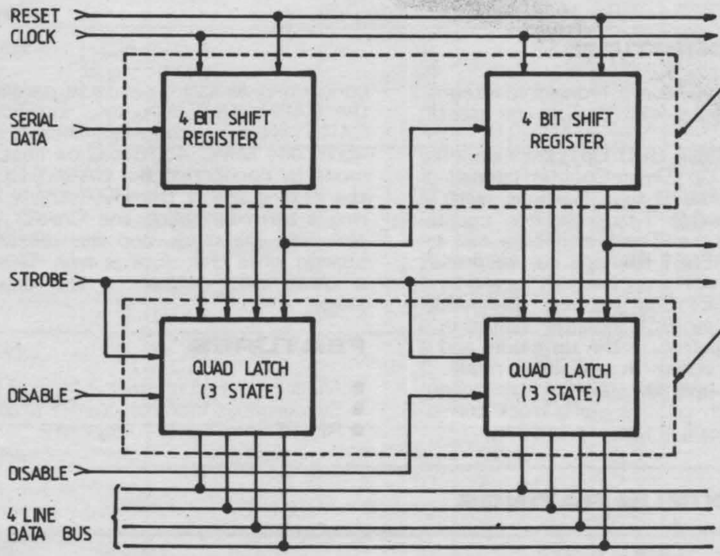
X = Don't care
Z = High impedance

TEST WAVEFORM

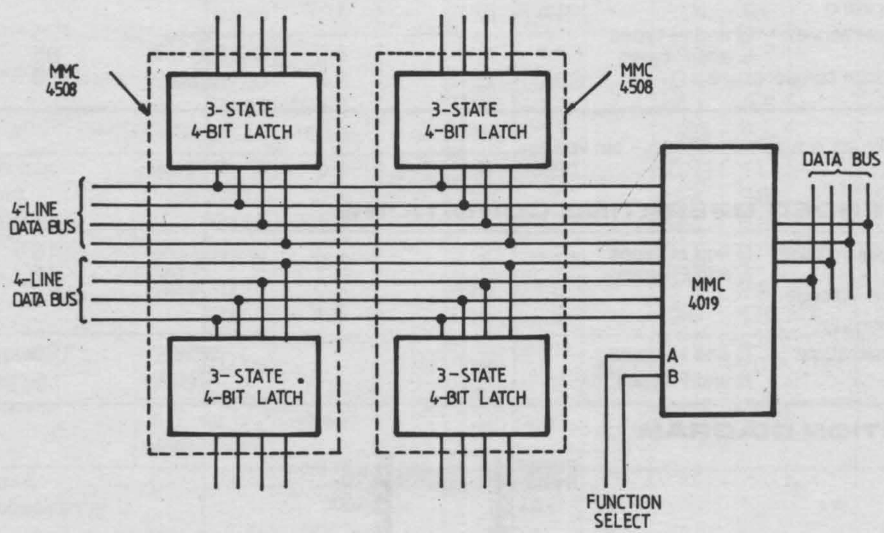


TYPICAL APPLICATIONS

Bus register



Dual multiplexed bus register with function select



PRESETTABLE UP/DOWN COUNTERS:
MMC 4510 PRESETTABLE BCD UP/DOWN COUNTERS
MMC 4516 PRESETTABLE BINARY UP/DOWN COUNTER

GENERAL DESCRIPTION

The MMC 4510, MMC 4516 are monolithic integrated circuits available in 16-lead dual in-line plastic package.
The MMC 4510 Presetable BCD Up/Down Counter and MMC 4516 Binary Up/Down Counter consist of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters. These counters can be cleared by a high level RESET line, and can be preset to any binary number present on the jam inputs by a high level on the PRESET ENABLE line. The MMC 4510 will count out of non-BCD counter states in a maximum of two clock pulses in the up mode, and a maximum of four clock pulses in the down mode. If the CARRY-IN input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the CARRY-OUT of a less significant stage to the CARRY-IN of a more significant stage. The MMC 4510 and MMC 4516 can be cascaded in the ripple mode by connecting the CARRY-OUT to the clock of the next stage. If the UP/DOWN input changes during a terminal count, the CARRY-OUT must be gated with the clock, and the UP/DOWN input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage.

FEATURES

- Medium speed operation f_{c1} = 8 MHz typ. at 10 V
- Synchronous internal CARRY propagation
- RESET and PRESET capability

ABSOLUTE MAXIMUM RATINGS

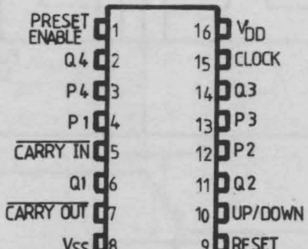
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature:	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Imput voltage		0 to	V_{DD}	V
T_A	Operating temperature:	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15	Any input		15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

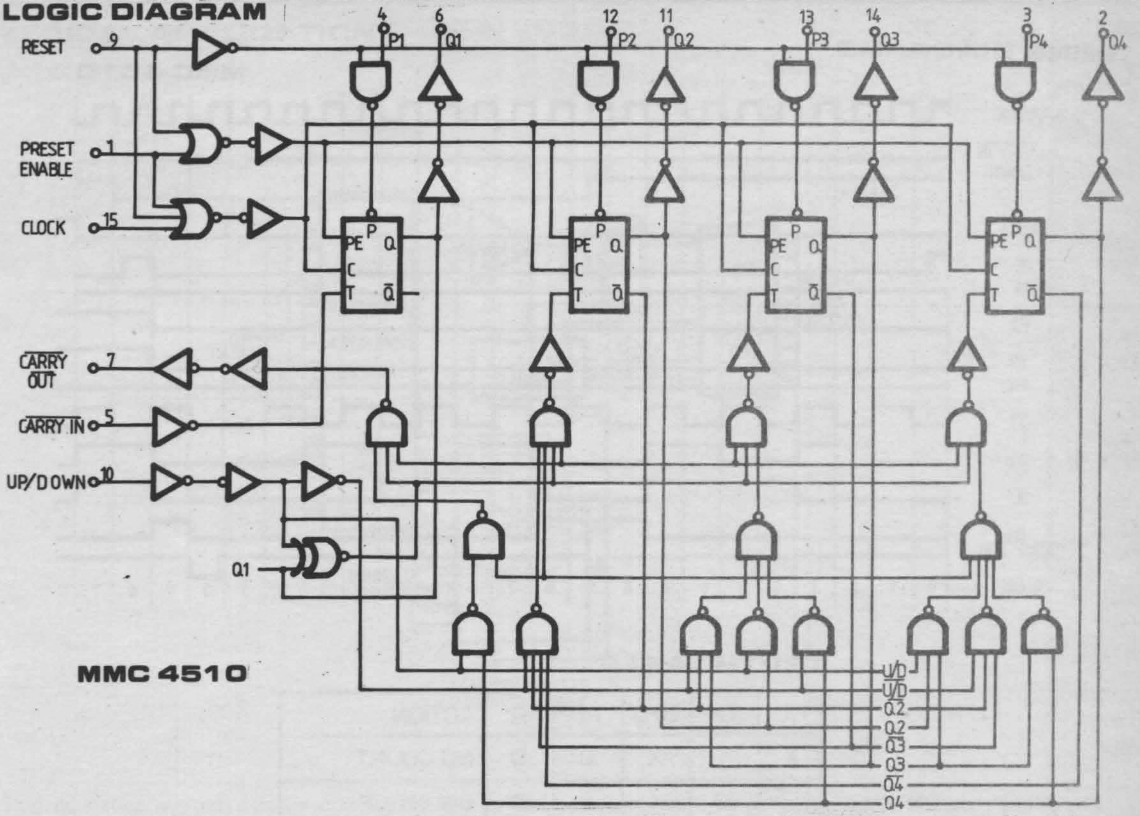
DYNAMIC ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C, C_L = 50 pF, R_L = 200 k, typical temperature coeficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

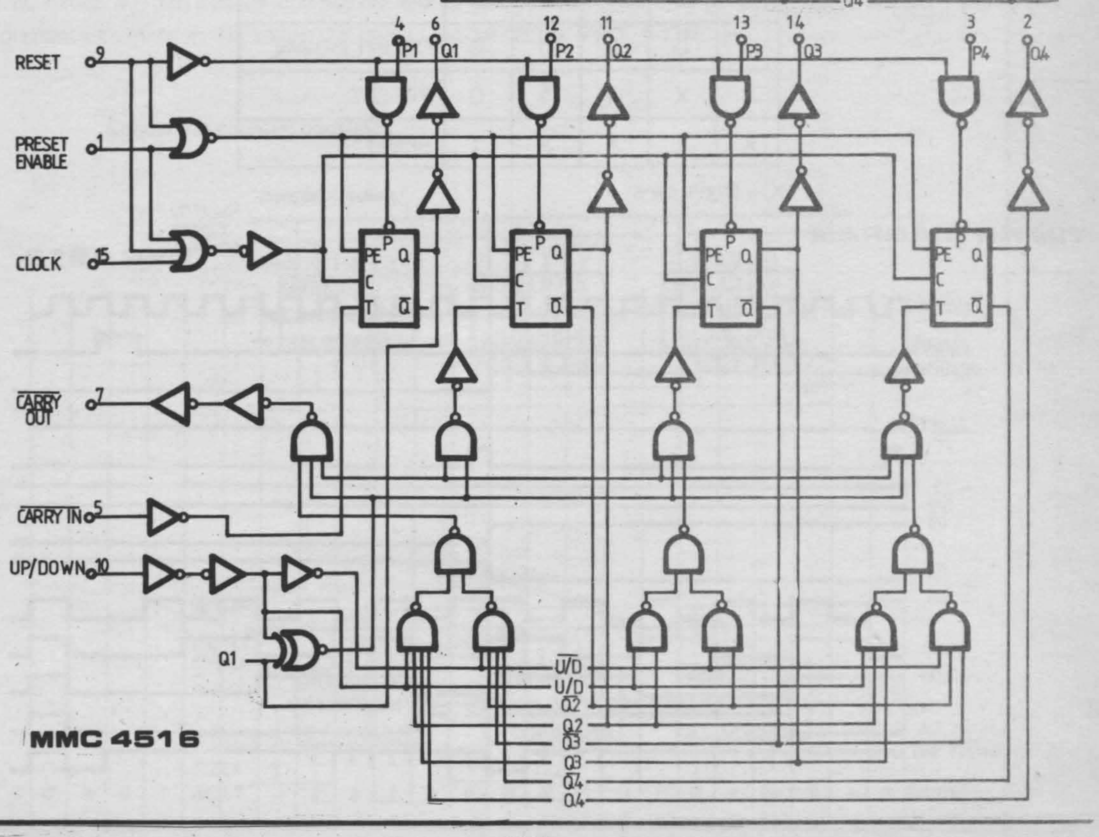
	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES			UNIT
			MIN.	TYP.	MAX.	
t_{PHL}, t_{PLH}	Propagation delay time Clock to Q	5 10 15		200 100 75	400 200 150	ns
t_{PHL}, t_{PLH}	Propagation delay time preset or reset to Q output	5 10 15		210 105 80	420 210 160	ns
t_{PHL}, t_{PLH}	Propagation delay time clock to carry out	5 10 15		240 120 90	480 240 180	ns
t_{PHL}, t_{PLH}	Propagation delay time carry in to carry out	5 10 15		125 60 50	250 120 100	ns
t_{PHL}, t_{PLH}	Propagation delay time preset or reset to carry out	5 10 15		320 160 125	640 320 250	ns
t_{TLH}, t_{THL}	Transition time	5 10 15		100 50 40	200 100 80	ns
f_{max}	Max. clock frequency	5 10 15	2 4 5.5	4 8 11		MHz
t_W	Clock pulse width	5 10 15	150 75 60			ns
	(°) Preset enble or removal time	5 10 15	150 80 60			ns
t_r, t_f	✲ Clock rise and fall time	5 10 15			15 5 5	ns
t_{setup}	Carry in setup time	5 10 15	130 60 45			ns
t_{setup}	Up-down setup time	5 10 15	360 160 110			ns
t_W	Preset enable or reset pulse width	5 10 15	220 100 75			ns

(°) Time required after the falling edge of the reset or preset enable inputs before the rising edge of the clock will trigger the counter (similar to setup time).
✲ If more than unit is cascaded in the parallel clocked application, t_r clock should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.

LOGIC DIAGRAM



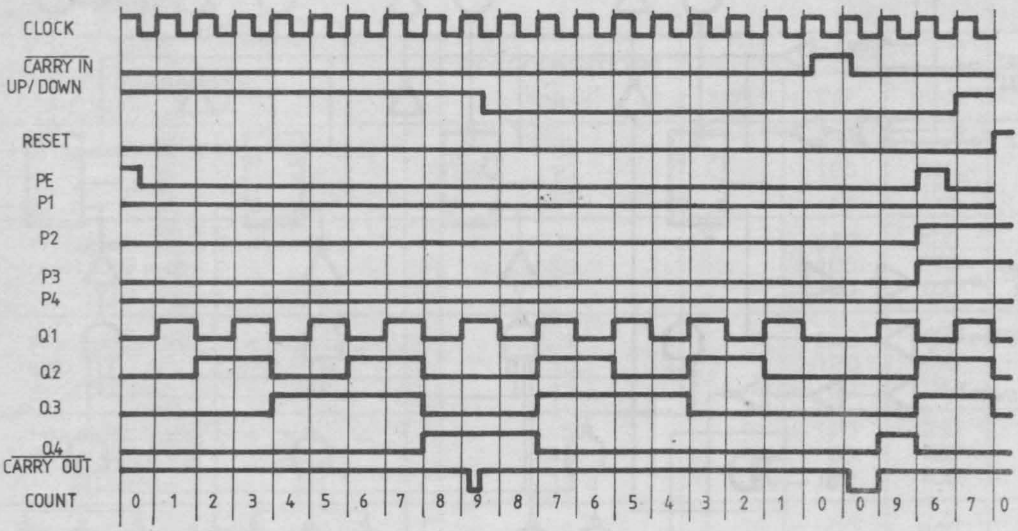
MMC 4510



MMC 4516

TIMING DIAGRAMS

MMC 4510



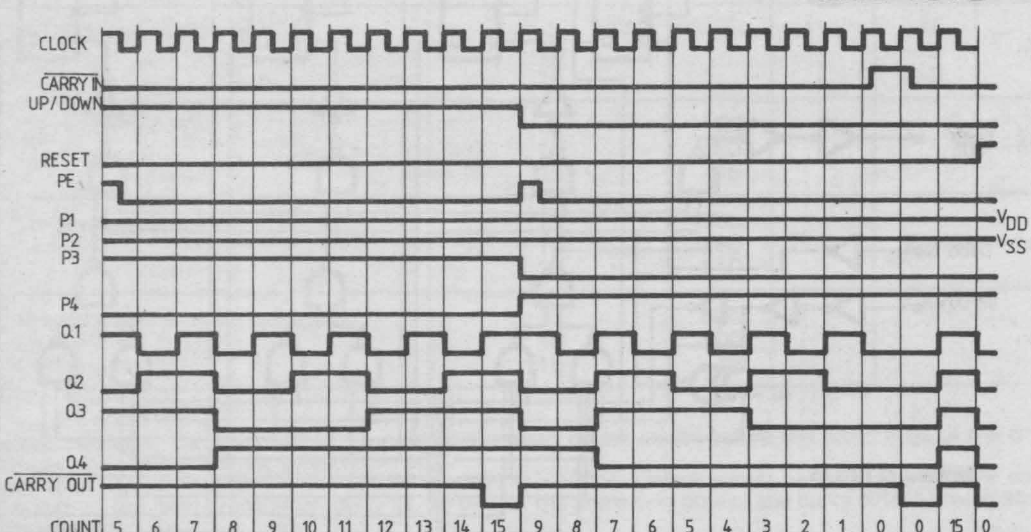
TRUTH TABLE

CL	CI	U/D	PE	R	ACTION
X	1	X	0	0	NO COUNT
_⌈	0	1	0	0	COUNT UP
_⌈	0	0	0	0	COUNT DOWN
X	X	X	1	0	PRESET
X	X	X	X	1	RESET

X = Don't care

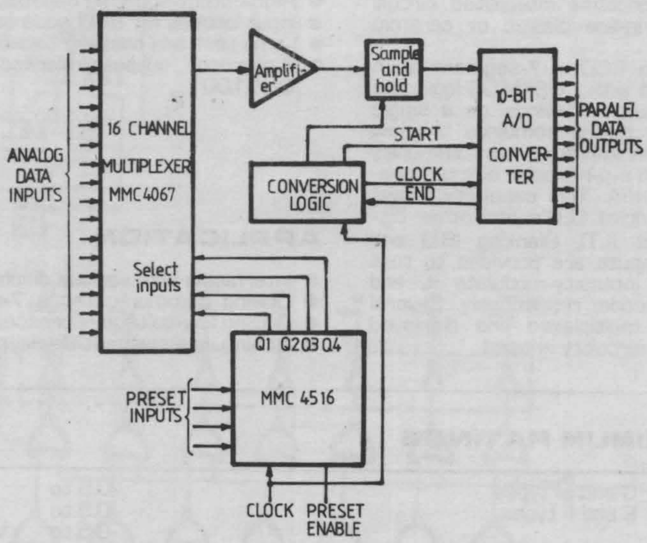
TIMING DIAGRAM

MMC 4516



TYPICAL APPLICATIONS

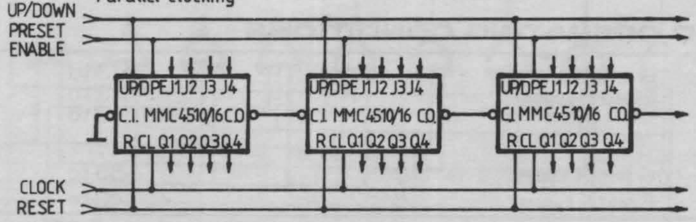
Typical 16-channel 10 bit data aquisition system



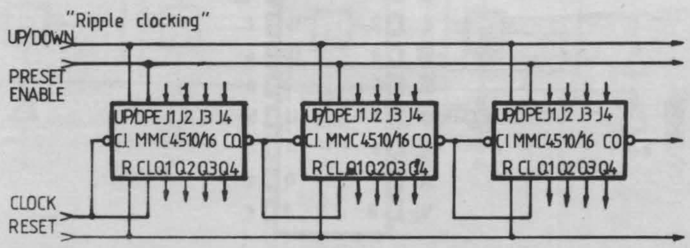
This aquisition system can be operated in the random access mode by jamming in the channel number at the present inputs, or in the sequential mode by clocking the MMC 4516.

Cascading counter packages

"Parallel clocking"



"Ripple clocking"



BCD-TO-SEVEN SEGMENT LATCH/ DECODER/DRIVER

GENERAL DESCRIPTION

The MMC 4511 is a monolithic integrated circuit available in 16-lead dual in-line plastic or ceramic package

The MMC 4511 type is a BCD-to-7-segment latch decoder driver constructed with COS/MOS logic and n-p-n bipolar transistor output devices on a single monolithic structure. This device combines the low quiescent power dissipation and high noise immunity features of COS/MOS with n-p-n bipolar output capable of sourcing up to 25 mA. This capability allows the MMC 4511 type to drive LED's and other displays directly. Lamp Test (LT), Blanking (BL) and Latch Enable or Strobe inputs are provided to test the display, shut off or intensity-modulate it, and store or strobe a BCD code, respectively. Several different signals may be multiplexed and displayed when external multiplexing circuitry is used.

FEATURES

- High-output-sourcing capability (up to 25mA)
- Input latches for BCD code storage
- Lamp test and blanking capability
- 7-segment outputs blanked for BCD input codes > 1001

APPLICATION

- Interfacing with various displays
- Driving common-cathode 7-segment LED displays
- Driving low-voltage fluorescent displays
- Driving incandescent displays.

ABSOLUTE MAXIMUM RATINGS

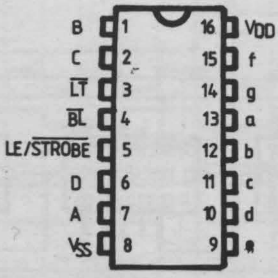
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

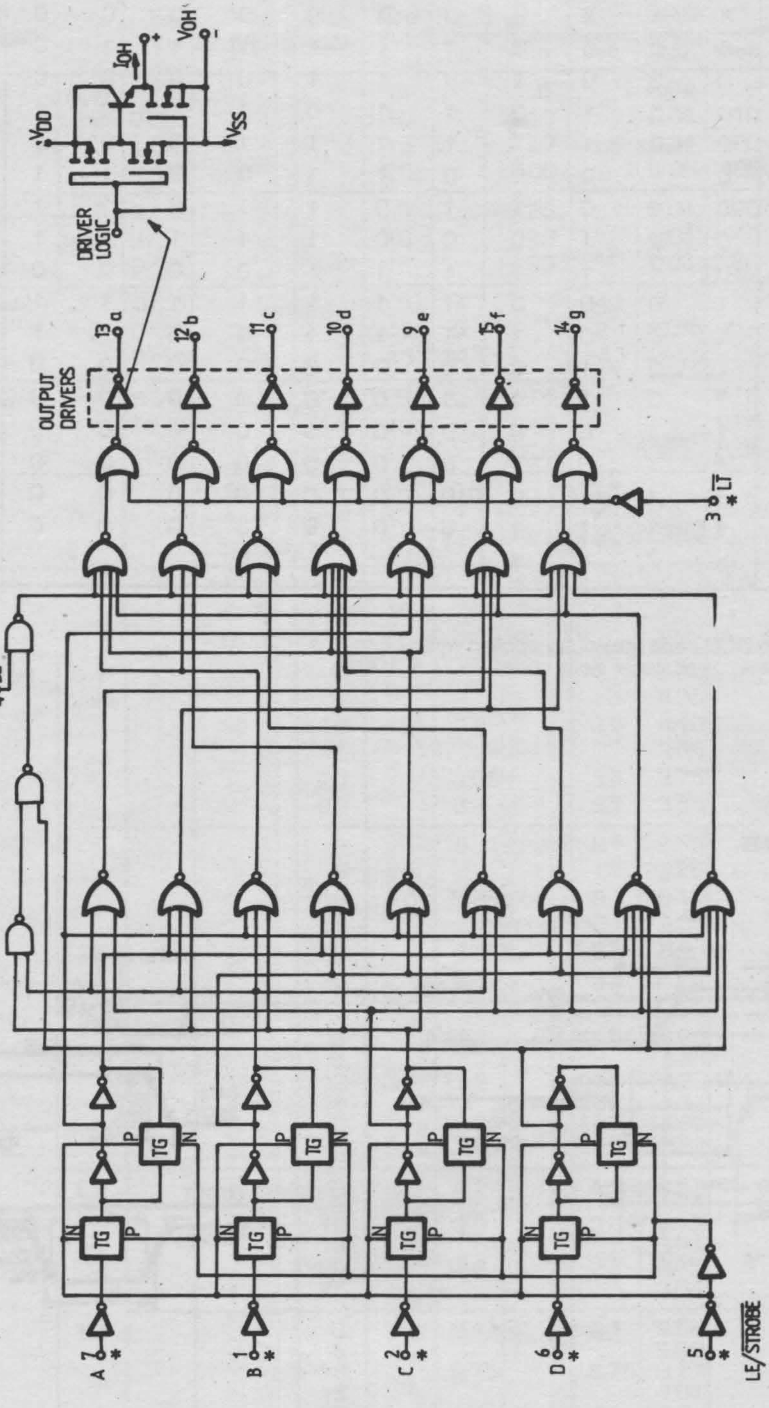
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



LOGIC DIAGRAM

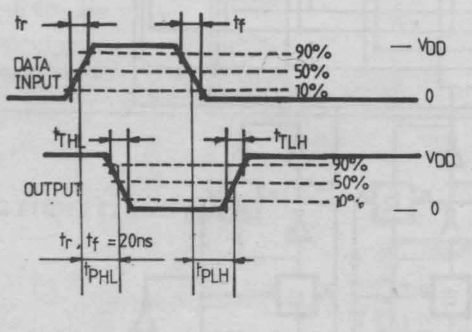


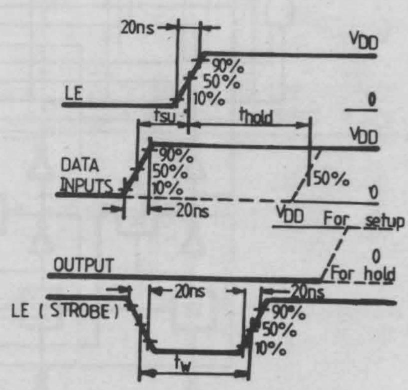
TRUTH TABLE

LE	BI	LT	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X				✲				✲

X = Don't care
✲ = Depends on BCD code previously applied when LE = 0
Note : Display is blank for all illegal input codes (BCD > 1001)

WAVEFORMS





STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5			5	4		4.1	4.55		4.2		V
			0/10			10	9		9.1	9.55		9.2		
			0/15			15	14		14.1	14.55		14.2		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
V_{OH}	Output drive voltage	G, H types			0		4.1		4.1	4.55		4.2		V
					5					4.25				
					10	5	3.8		3.9	4.10		3.9		
					15					3.95				
					20		3.55		3.4	3.75				
					25		3.4		3.1	3.55				
					0		9		9.1	9.55		9.2		V
					5					9.25				
					10	10	8.85		9	9.15				
					15					9.05				
					20		8.7		8.6	8.9		8.4		
					25		8.6		8.3	8.75				
					0		14		14.1	14.55		14.2		V
					5					14.3				
					10	15	13.9		14	14.2		14.0		
					15					14.1				
					20		13.75		13.7	13.95		13.5		
					25		13.65		13.5	13.8		13.1		
		E, F types			0		4.1		4.1	4.57		4.1		V
					5					4.24				
					10		3.6		3.6	4.12		3.3		
					15	5				3.94				
					20		2.8		2.8	3.75		2.5		
					25					3.54				
					0		9.1		9.1	9.58		9.1		V
					5					9.26				
					10		8.75		8.75	9.17		8.45		
					15	10				9.04				
					20		8.1		8.1	8.9		7.8		
					25					8.75				

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
		E, F types			0	15	14.1		14.1	14.59		14.1		V
					5					14.27				
					10		13.75		13.75	14.18		13.45		
					15					14.07				
					20		13.1		13.1	13.95		12.8		
					25					13.8				
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		±10^{-5}	±0.1		±1	μA
		E, F types	0/15			15		±0.3		±10^{-5}	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:
1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

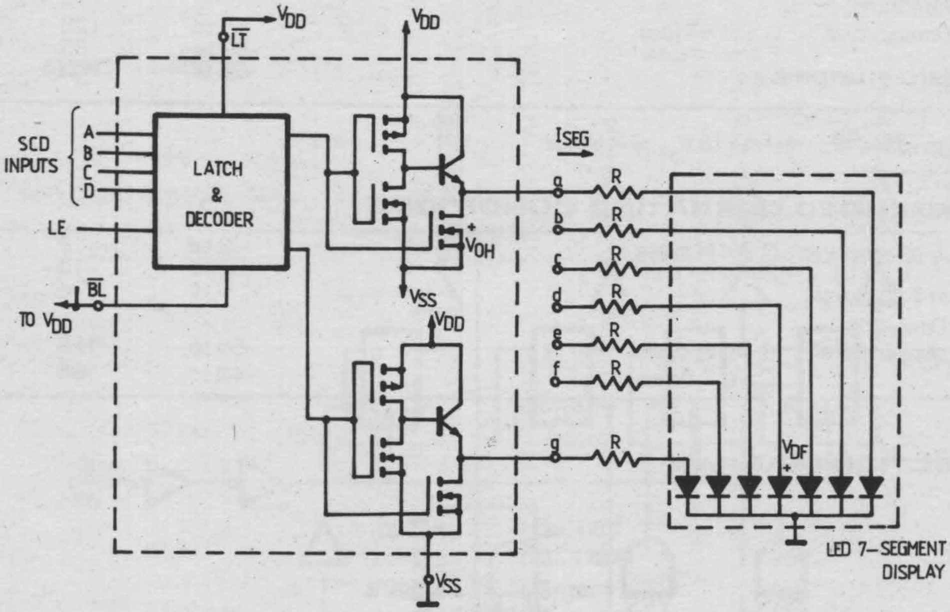
(T_A = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

PARAMETER		TEST CONDITIONS V_{DD}(V)	VALUES min.	typ.	max.	UNIT
t_{PHL}	Propagation delay time (Data)	5		520	1040	ns
		10		210	420	
		15		150	300	
t_{PLH}	Propagation delay time (Data)	5		660	1320	ns
		10		260	520	
		15		180	360	
t_{PHL}	Propagation delay time ($\overline{BL}$)	5		350	700	ns
		10		175	350	
		15		150	300	
t_{PLH}	Propagation delay time ($\overline{BL}$)	5		400	800	ns
		10		175	350	
		15		150	300	
t_{PHL}	Propagation delay time ($\overline{LT}$)	5		250	500	ns
		10		125	250	
		15		85	170	
t_{PLH}	Propagation delay time ($\overline{LT}$)	5		150	300	ns
		10		75	150	
		15		50	100	

PARAMETER		TEST CONDITIONS VDD(V)	VALUES min.	typ.	max.	UNIT
t_{TLH}	Transition time	5 10 15		40 30 20	80 60 50	ns
t_{THL}	Transition time	5 10 15		125 75 65	310 185 160	ns
t_{setup}	Setup time	5 10 15	150 70 40	75 35 20		ns
t_{hold}	Hold time	5 10 15	0 0 0	-75 -35 -20		ns
t_W	Strobe pulse width	5 10 15	400 160 100	200 80 50		ns

APPLICATION

Driving common-cathode 7-segment LED displays



DUAL UP-COUNTERS: MMC 4518 DUAL BCD UP-COUNTER MMC 4520 DUAL BINARY UP-COUNTER

GENERAL DESCRIPTION

The MMC 4518/4520 are monolithic integrated circuits available in 16-lead dual in-line plastic package.
The MMC 4518 Dual BCD Up Counter and MMC 4520 Dual Binary Up Counter each consist of two identical, internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition. For single-unit operation the Enable input is maintained „high" and the counter advances on each positive-going transition of the Clock. The counters are cleared by high levels on their Reset lines. The counter can be cascaded in the ripple mode by connecting Q4 to the Enable input of the subsequent counter while the clock input of the latter is held low.

FEATURES

- Medium-speed operation-6 MHz typ. clock frequency at 10 V
- Positive or negative edge triggering
- Synchronous internal CARRY propagation

ABSOLUTE MAXIMUM RATINGS

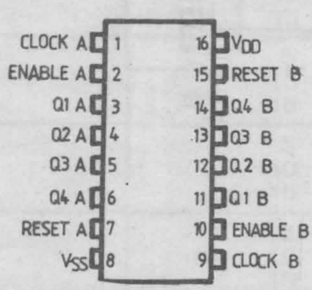
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

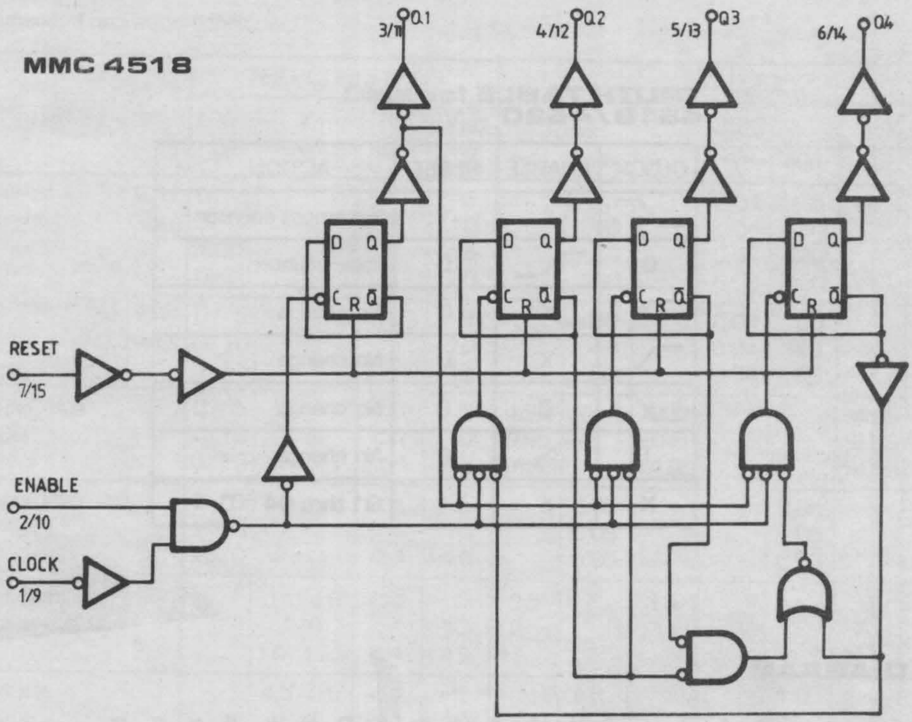
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Imput voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM

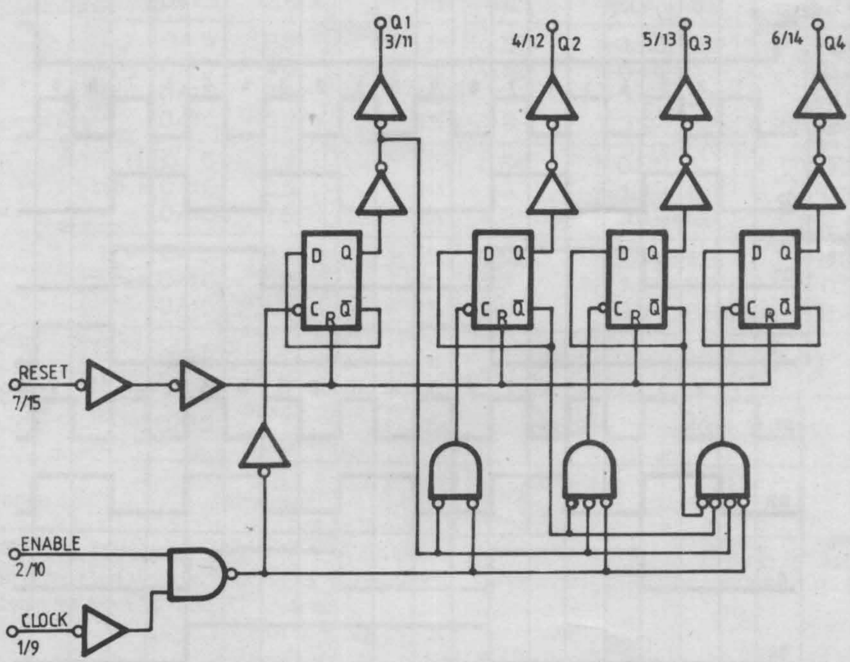


LOGIC DIAGRAM

MMC 4518



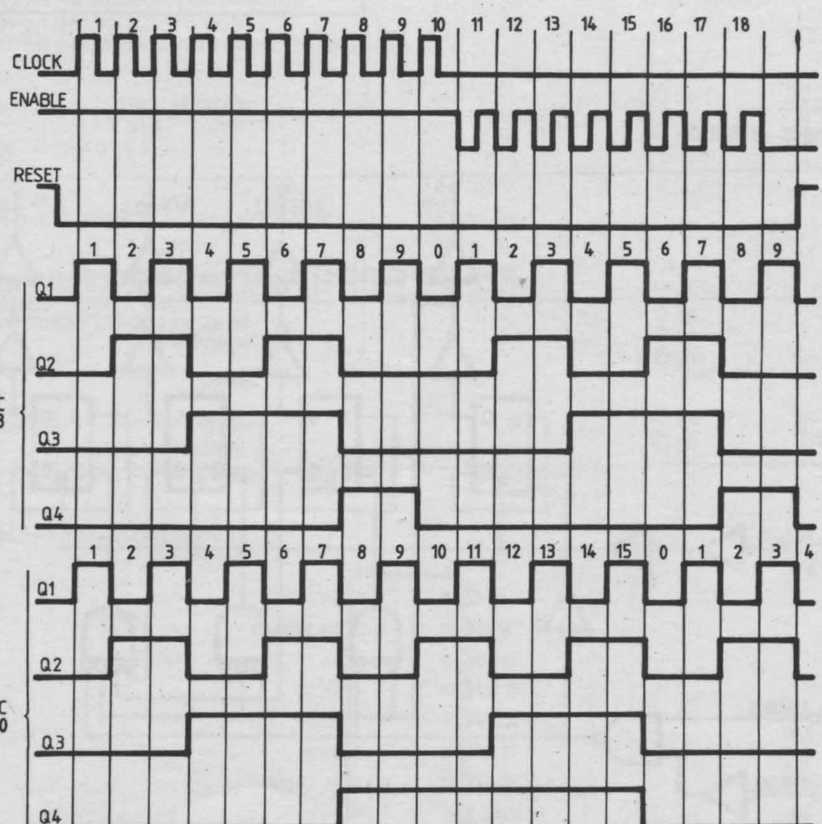
MMC 4520



TRUTH TABLE for MMC 4518/4520

CLOCK	ENABLE	RESET	ACTION
↑	1	1	Increment counter
0	↓	0	Inter counter
X	↑	0	No change
↓	X	0	No change
↑	0	0	No change
1	↓	0	No change
X	X	1	Q1 thru Q4 = 0

TIMING DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V

2 V min. with V_{DD} = 10 V

2.5 V min. with V_{DD} = 15 V

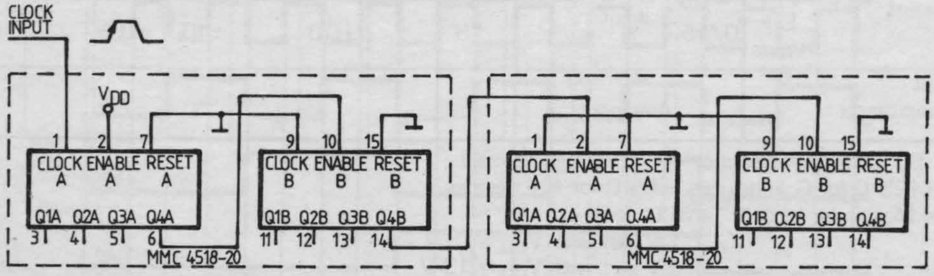
DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 k, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20 ns)

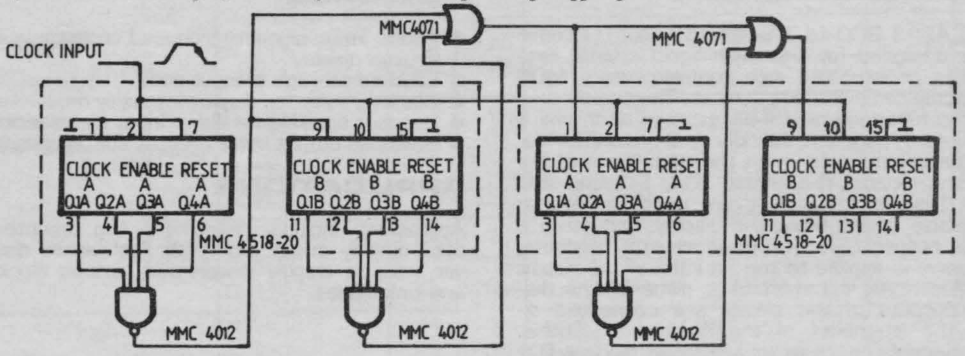
PARAMETER		TEST CONDITIONS V_{DD}(V)	VALUES			UNIT
			Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	propagation delay time (Reset to output)	5 10 15		280 115 80	560 230 160	ns
t_{PLH}, t_{PHL}	Propagation delay time (Clock or Enable to output)	5 10 15		330 130 90	650 225 170	ns
t_{TLH}, t_{THL}	Transition time	5 10 15		100 50 40	200 100 80	ns
t_W,	Clock pulse width	5 10 15	200 100 70	100 50 35		ns
t_W,	Enable pulse width	5 10 15	400 200 140	200 100 70		ns
t_r, t_f	Clock or enable rise and fall time	5 10 15			15 15 5	μs
f_{max},	Maximum clock frequency	5 10 15	1.5 3 4	3 6 8		MHz
t_r, t_f	Clock input rise and fall time	5 10 15			15 5 5	μs
t_W,	Reset pulse width	5 10 15	250 110 80	125 55 40		ns

TYPICAL APPLICATIONS

Ripple cascading of four counters with positive-edge triggering



Synchronous cascading of four binary counters with negative-edge triggering



BCD-TO-SEVEN SEGMENT LATCH/ DECODER/DRIVER

GENERAL DESCRIPTION

The MMC 4543 BCD-to-7 Segment Latch/Decoder /Driver is designed for use with liquid crystal readouts and is constructed with complementary MOS (CMOS) enchancement-mode devices. The circuit provides the functions of a 4-bit storage latch and a 8421 BCD-to 7 segment decoder and driver. The device has the capability to invert the logic levels of the output combinations. The Phase (Ph), Blanking (BI), and Latch Disable (LD) inputs are used to reverse the truth-table phase, blank the display, and store a BCD code, respectively. For liquid crystal readouts, a square wave is applied to the Ph input of the circuit and the electrically common back plane of the display. The outputs of the circuit are connected directly to the segments of the readout. For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connections diagrams are given on this data sheet

FEATURES

- Phase input signal reproduced on outputs for liquid crystal display
- Latched storage of input code
- Blanking input for display intensity modulation
- Readout blanking for illegal input combinations
- Balanced output drive current specifications

APPLICATIONS

Aplications include instrument (e.g. counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

ABSOLUTE MAXIMUM RATINGS

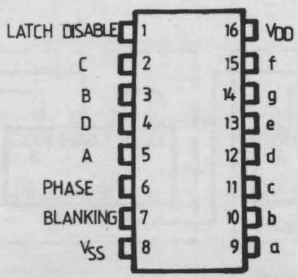
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V

2 V min. with V_{DD} = 10 V

2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

($C_L = 5$ pF, $T_A = 25°C$)

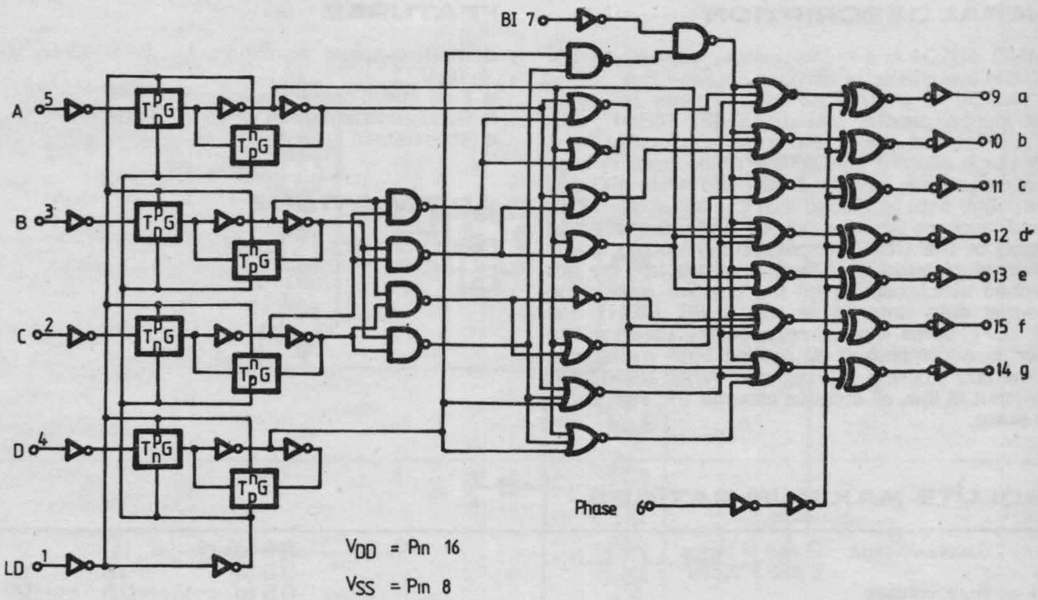
PARAMETER	V_{DD} (Vdc)	VALUES min.	VALUES typ.	VALUES max.	UNIT
t_{PHL}, t_{PLH} Propagation delay time	5 10 15		550 210 160	1100 420 320	ns
t_{TLH}, t_{THL} Output transition time	5 10 15		100 50 40	200 100 80	ns
t_{setup} Minimum data input setup time	5 10 15		−40 −15 −10	0 0 0	ns
t_{hold} Minimum data input hold time	5 10 15		40 15 10	80 30 20	ns
PW_{LD} Minimum LD pulse width	5 10 15		125 50 40	250 100 80	ns

TRUTH TABLE

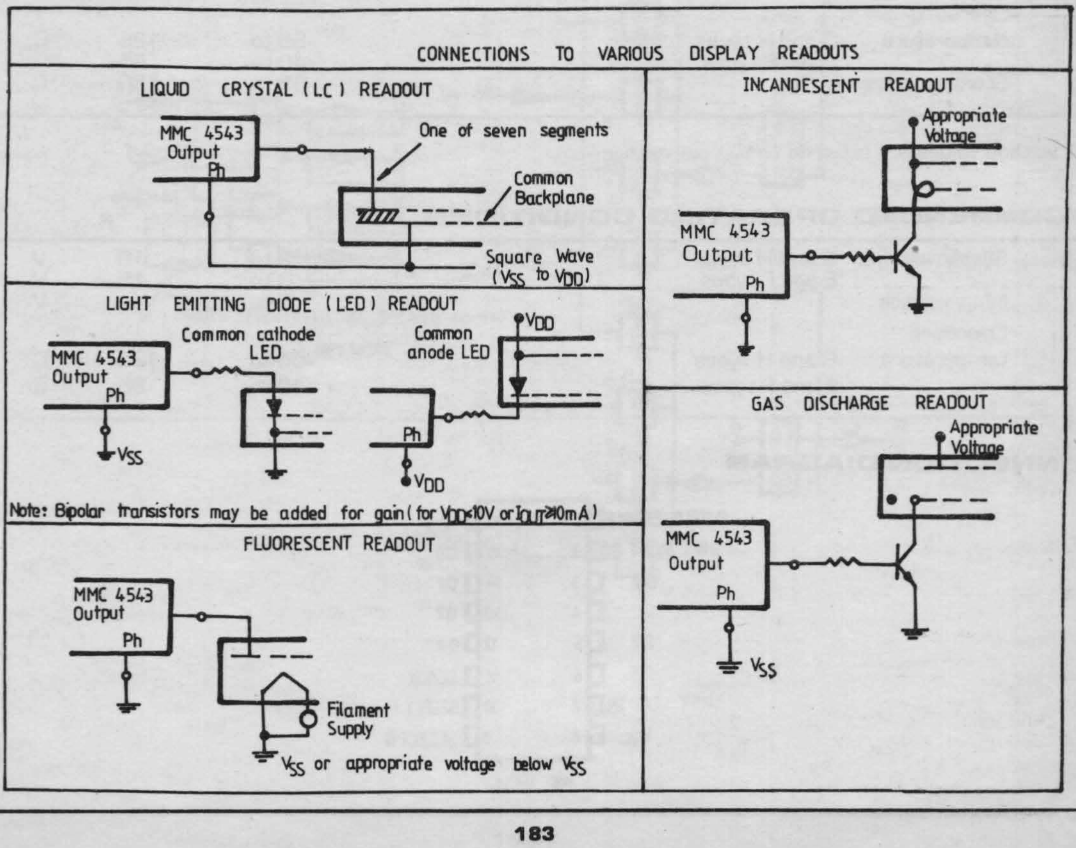
INPUTS							OUTPUTS							
LD	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	1	0	X	X	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	1	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	0	1	1	1	1	1	0	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	1	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X			*		*			* *
†	†	1	†				Inverse of output combinations above							Display as above

X = Don't care
† = Above combinations
* = For liquid crystal readouts, apply a square wave to Ph
For common cathode LED readouts, select Ph = 0
For common anode LED readous, select Ph = 1
** = Depends upon the BCD code previously applied when LD = 1

LOGIC DIAGRAM



TYPICAL APPLICATIONS



4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

GENERAL DESCRIPTION

The MMC 40104 is a monolithic i.c., available in 16-lead dual in-line plastic or ceramic package The MMC 40104 is a universal shift register featuring parallel inputs, parallel outputs, SHIFT RIGHT and SHIFT LEFT serial inputs, and a high-impedance third output state allowing the device to be used in bus-organized systems. In the parallel-load mode (SO and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift-right and shift-left are accomplished synchronously on the positive clock edge with serial data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clearing the register is accomplished by setting both mode controls low and clocking the register When the output enable input is low, all outputs assume the high impedance state.

FEATURES

- Medium-speed operation: f_{CL} = 9 MHz, V_{DD} = 10 V
- Fully static operation
- Synchronous parallel or serial operation
- Three-state outputs

APPLICATIONS

Control circuitry

ABSOLUTE MAXIMUM RATINGS

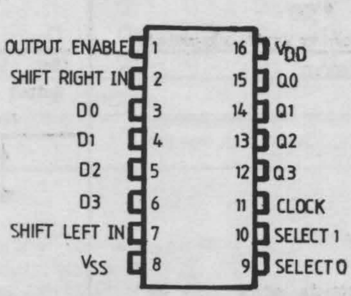
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

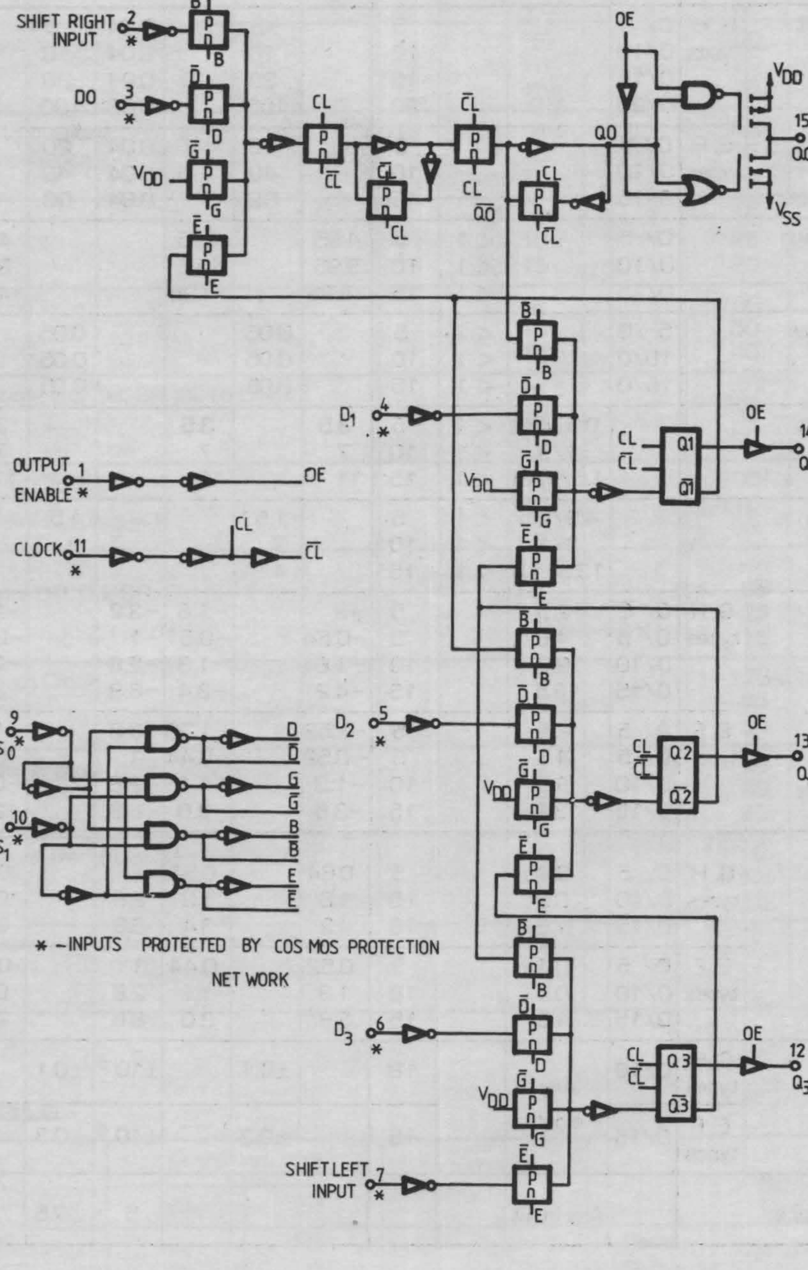
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



TOP VIEW

LOGIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
		E, F types	0/15	Any input		15		±0.3		$\pm 10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55$°C for G, H devices; -40°C for E, F devices.

* $T_{HIGH} = +125$°C for G, H devices; $+85$°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V
2 V min. with $V_{DD} = 10$ V
2.5 V min. with $V_{DD} = 15$ V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20 ns).

	PARAMETER	TEST CONDITIONS V_{DD}(V)	VALUES min.	VALUES typ.	VALUES max.	UNIT
t_{PLH}, t_{PHL}	Propagation delay time Clock to Q	5		220	440	ns
		10		100	200	
		15		70	140	
t_{PZH}, t_{PZL}, t_{PLZ}	3—state outputs High impedance	5		80	160	ns
		10		35	70	
		15		25	50	
t_{PHZ}		5		45	90	ns
		10		25	50	
		15		20	40	
t_{THL}, t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
t_{setup}	Setup time D0, D3, SR, SL to Clock	5		80	100	ns
		10		35	70	
		15		20	50	
	S0, S1 to Clock	5		200	400	ns
		10		110	220	
		15		65	130	
t_{hold}	Hold time D0, D3, SR, SL	5		−65	0	ns
		10		−25	0	
		15		−15	0	
	S0, S1 to Clock	5		−170	0	ns
		10		−95	0	
		15		−55	0	
t_w	Clock pulse width	5		90	180	ns
		10		40	180	
		15		25	50	
f_{CL}	Clock input frequency	5	3	6		MHz
		10	6	12		
		15	8	15		
t_r, t_f	Clock input rise or fall time	5			1000	μs
		10			100	
		15			100	

TRUTH TABLE

CLOCK	MODE SELECT S0	MODE SELECT S1	OUTPUT ENABLE	ACTION
	0	0	1	Reset
	1	0	1	Shift right (Q0 toward Q3)
	0	1	1	Shift left (Q3 toward Q0)
	1	1	1	Parallel load
x	x	x	0	Operations occur as shown above, but outputs assume high impedance

DUAL 2-INPUT NAND BUFFER/DRIVER

GENERAL DESCRIPTION

The MMC 40107 is a monolithic i.c., available in 14-lead dual in-line ceramic package and plastic package.
The MMC 40107 is a dual 2-input NAND buffer/driver containing two independent 2-input NAND buffers with open-drain single n-channel transistor outputs
This device features a wired-OR capability and high output sink current capability (136 mA typ at V_{DD} = 10 V, V_{DS} = 1 V)

FEATURES

- quiescent current specified to 20 V
- maximum input leakage of 1 μA at 18 V (full package temperature range)
- standardized symmetrical output characteristics
- 5 V, 10 V, and 15 V parametric ratings

APPLICATIONS

.Driver circuits

ABSOLUTE MAXIMUM RATINGS

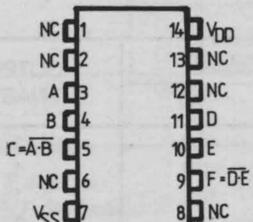
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS				VALUES							UNIT
		V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	
		0/10			10		2		0.02	2		60	
		0/15			15		4		0.02	4		120	
		0/20			20		20		0.04	20		600	μA
	E, F types	0/ 5			5		4		0.02	4		30	
		0/10			10		8		0.02	8		60	
		0/15			15		16		0.02	16		120	
V_{IH}** Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		
			1/9	< 1	10	7		7			7		V
			1.5/13.5	< 1	15	11		11			11		
V_{IL}** Input low voltage			4.5	< 1	5		1.5			1.5		1.5	
			9	< 1	10		3			3		3	V
			13.5	< 1	15		4			4		4	
I_{OL} Output sink current	G, H types	5	0.4		5	21		16	32		12		
		5	1		5	44		30	68		25		
		10	0.5		10	49		37	74		28		
		10	1		10	89		68	136		51		
		15	0.5		15	66		50	100		38		
	E, F types	5	0.4		5	17		13.6	32		12		
		5	1		5	35.7		25.5	68		22		
		10	0.5		10	39.1		31.4	74		27		
		10	1		10	72.2		57.8	136		51		
		15	0.5		15	53.5		42.5	100		37		
I_{OH} Output drive current		No internal pull-up device											mA
I_{IH}, I_{IL} Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
	E, F types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		±1	
I_{OH}, I_{OL}*** 3-state output leakage current	G, H types	0/18	18		18		2		10^{-4}	2		20	μA
	E, F types	0/15	15		15		2		10^{-4}	2		20	
C_I Input capacitance		Any input							5	7.5			pF
C_O Output capacitance		Any output							30				

* $T_{LOW} = -55$°C for G, H devices; -40°C for E, F devices.
* $T_{HIGH} = +125$°C for G, H devices; $+85$°C for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with $V_{DD} =$ 5 V
2 V min. with $V_{DD} =$ 10 V
2.5 V min. with $V_{DD} =$ 15 V

** Measured with external pull-up resistor, $R_L = 10\ K\Omega$ to V_{DD}

*** Forced output disabled

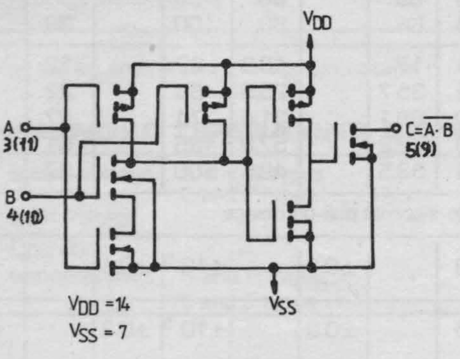
DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20 ns)

PARAMETER		TEST CONDITIONS		VALUES			UNIT
			V_{DD}(V)	min.	typ.	max.	
t_{PHL}, t_{PLH}	Propagation delay time High-to-Low	R_L*=120 Ω	5 10 15		100 45 30	200 90 60	ns
	Low-to-High	R_L*=120 Ω	5 10 15		100 60 50	200 120 100	ns
t_{THL} t_{TLH}	Transition time High-to-Low	R_L*=120 Ω	5 10 15		50 20 10	100 40 20	ns
	Low-to-High	R_L*=120 Ω	5 10 15		50 35 25	100 70 50	ns

*R_L is external pull-up resistor to V_{DD}.

SCHEMATIC DIAGRAM AND TRUTH TABLE



TRUTH · TABLE

A	B	C	
0	0	1*	Z#
1	0	1*	Z#
0	1	1*	Z#
1	1	0	

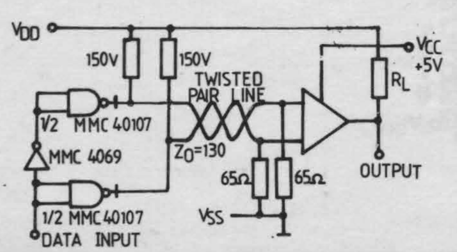
* Requires external pull-up resistor (R_L) to V_{DD}.

Without pull-up resistor (3-state)

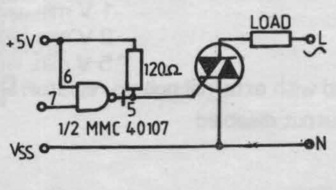
TYPICAL APPLICATIONS

The bar on the output line of this logic diagram indicates that the output is open drain as is shown in the previons schematic diagram and truth table.

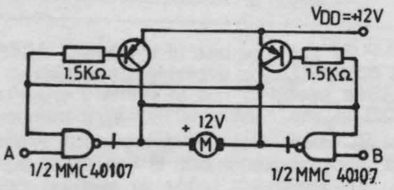
Line-driver circuit



Direct dc drive interface of 40107 with a triac

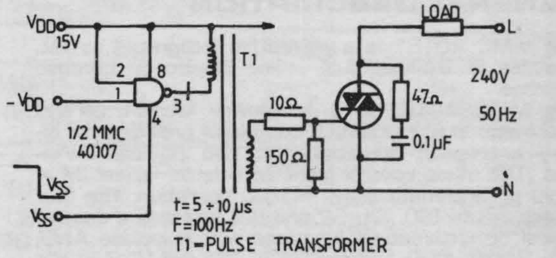


Motor-controller circuit

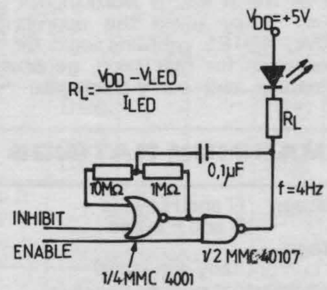


A	B	MOTOR FUNCTION
0	0	OFF
1	0	COUNTER CLOCKWISE
1	1	AS PREVIOUS STATE
0	1	CLOCKWISE
1	1	AS PREVIOUS STATE

Interface of 40107 with triac, whit COS/MOS component and triac isolated

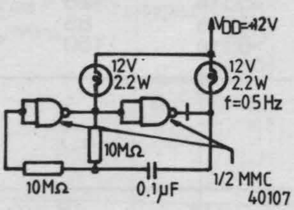


LED driver circuit

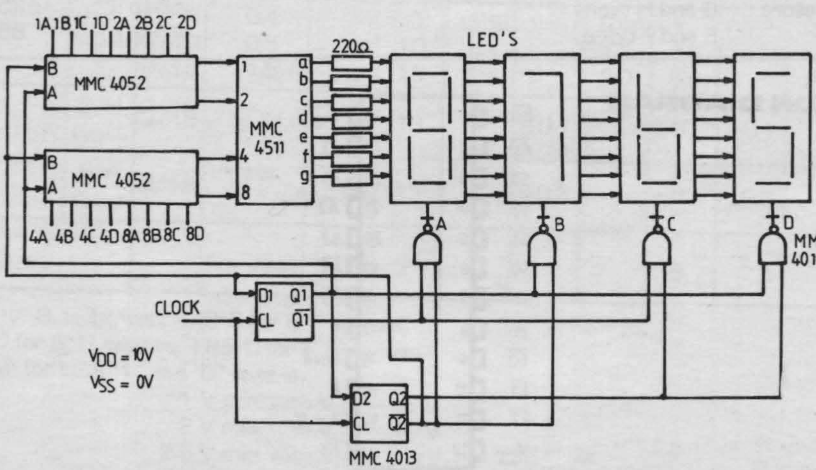


INHIBIT	ENABLE	OUTPUT
0	0	OFF
1	0	OFF
0	1	OFF
1	1	ON

A 2.2 watt incandescent lamp-driver circuit



Multiplexed LED circuit



4-BIT ARITHMETIC LOGIC UNIT

GENERAL DESCRIPTION

The MMC 40181 is a monolithic integrated circuit, available in 24-lead dual in-line plastic or ceramic package.
The MMC 40181 is a low-power four-bit parallel arithmetic logic unit (ALU) capable of providing 16 binary arithmetic operations on two Boolean variables. The mode control input M selects logical (M = High) or arithmetical (M = Low) operation. The four select inputs (S0, S1, S2 and S3) select the desired logical or arithmetical functions, which include AND, OR, NAND, NOR and exclusive -OR and-NOR in the logical mode, and addition, substraction, decrement, left-shift, and straight transfer in the arithmetic mode, according to the truth table. The MMC 40181 operation may be interpreted with either active-low or active-high data at the A and B word inputs and the function outputs F, by using the appropriate truth table. The MMC 40181 contains logic for full look-ahead carry operation for fast carry generation using the carry-generate and carry-propagate outputs $\overline{G}$ and $\overline{P}$ for the four bits of the MMC 40181. A ripple carry output C_{n+4} is available for use in systems where speed is not of primary importance. Also included in the MMC 40181 is a comparator output A = B, which assumes a high level whenever the four-bit input words A and B are equal and the device is in the substract mode. In addition, relative magnitude information may be derived from the carry-in input C_n and ripple carry-out output C_{n+4} by placing the unit in the substract mode and externally decoding using the information in Table II.

FEATURES

- Full look-ahead carry for speed operations on long words
- Generates 16 logic functions of two boolean variables
- Generates 16 arithmetic functions of two 4-bit binary words
- A = B comparator output avaible

ABSOLUTE MAXIMUM RATINGS

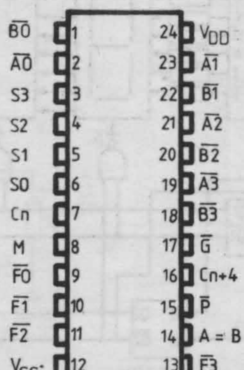
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	VALUES T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with $V_{DD} = 5$ V

2 V min. with $V_{DD} = 10$ V

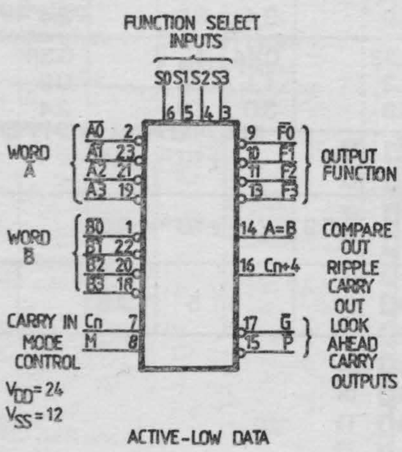
2.5 V min. with $V_{DD} = 15$ V

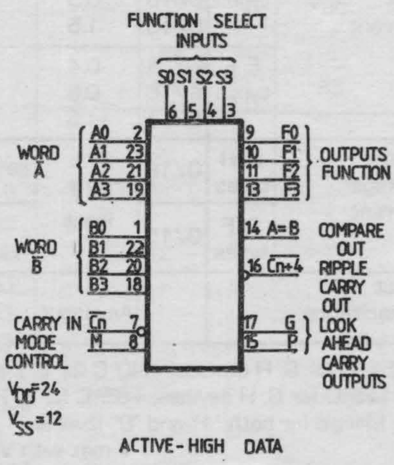
DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kΩ, typical temperature coefficient for all $V_{DD} = 0.3\%/°C$ all input rise and fall times = 20 ns).

	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES min.	VALUES typ.	VALUES max.	UNIT
t_{PLH} t_{PHL}	Propagation delay time A or B to F (logic mode) A or B to G or P	5		400	800	ns
		10		160	320	
		15		120	240	
	A or B to F, C_{n+4}, or A = B	5		300	1000	ns
		10		200	400	
		15		140	280	
	C_n to F	5		320	640	ns
		10		135	270	
		15		100	200	
	C_n to C_{n+4}	5		200	400	ns
		10		100	200	
		15		70	140	
t_{TLH}, t_{THL}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	

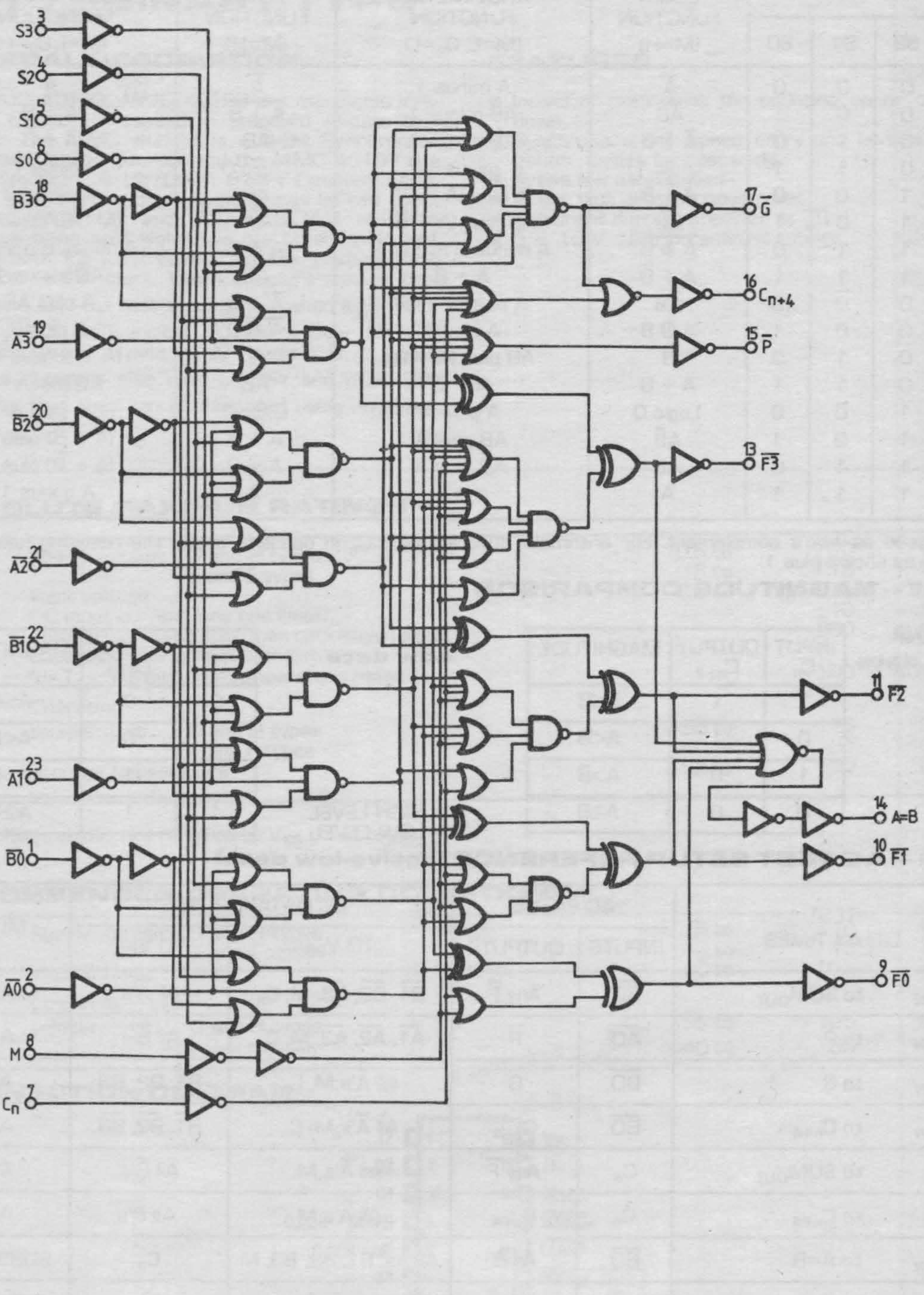
FUNCTIONAL DIAGRAM





LOGIC DIAGRAM

Active-low data



TRUTH TABLES Table I

FUNCTION SELECT				INPUTS/OUTPUTS ACTIVE LOW		INPUTS/OUTPUTS ACTIVE HIGH	
S3	S2	S1	S0	LOGIC FUNCTION (M=H)	ARITHMETIC* FUNCTION (M=L, C_n=L)	LOGIC FUNCTION (M=H)	ARITHMETIC* FUNCTION (M=L, $\overline{C_n}$=H)
0	0	0	0	$\overline{A}$	A minus 1	$\overline{A}$	A
0	0	0	1	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A + B
0	0	1	0	$\overline{A}+B$	$A\overline{B}$ minus 1	$\overline{A}B$	$A+\overline{B}$
0	0	1	1	Logic 1	minus 1	Logic 0	minus 1
0	1	0	0	$\overline{A+B}$	A plus $(A+\overline{B})$	$\overline{AB}$	A plus $A\overline{B}$
0	1	0	1	$\overline{B}$	AB plus $(A+\overline{B})$	$\overline{B}$	(A + B) plus $A\overline{B}$
0	1	1	0	$\overline{A\oplus B}$	A minus B minus 1	$A\oplus B$	A minus B minus 1
0	1	1	1	$A+\overline{B}$	$A+\overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
1	0	0	0	$\overline{A}B$	A plus (A + B)	$\overline{A}+B$	A plus AB
1	0	0	1	$A\oplus B$	A plus B	$\overline{A\oplus B}$	A plus B
1	0	1	0	B	$A\overline{B}$ plus (A + B)	B	$(A+\overline{B})$ plus AB
1	0	1	1	A + B	A + B	AB	AB minus 1
1	1	0	0	Logic 0	A plus A	Logic 1	A plus A
1	1	0	1	$A\overline{B}$	AB plus A	$A+\overline{B}$	(A + B) plus A
1	1	1	0	AB	$A\overline{B}$ plus A	A + B	$(A+\overline{B})$ plus A
1	1	1	1	A	A	A	A minus 1

* Expressed as two's complement. For arithmetic function with C_n in opposite state, the resulting function is as shown plus 1.

Table II — **MAGNITUDE COMPARISON**

Active-High data

INPUT C_n	OUTPUT C_{n+4}	MAGNITUDE
1	1	A≤B
0	1	A<B
1	0	A>B
0	0	A≥B

Active-Low data

INPUT C_n	OUTPUT C_{n+4}	MAGNITUDE
0	0	A≤B
1	0	A<B
0	1	A>B
1	1	A≥B

1 = HIGH LEVEL
0 = LOW LEVEL

Table III — **AC TEST SETUP REFERENCE (active-low data)**

TEST DELAY TIMES		AC PATHS		DC DATA INPUTS		MODE*
		INPUTS	OUTPUTS	TO V_{SS}	TO V_{DD}	
SUM_{IN}	to SUM_{OUT}	$\overline{B0}$	Any $\overline{F}$	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$, M, C_n	All $\overline{A}$'s	ADD
SUM_{IN}	to P	$\overline{A0}$	$\overline{P}$	$\overline{A1}$, $\overline{A2}$, $\overline{A3}$, M, C_n	All $\overline{B}$'s	ADD
SUM_{IN}	to G	$\overline{B0}$	$\overline{G}$	All $\overline{A}$'s, M, C_n	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$	ADD
SUM_{IN}	to C_{n+4}	$\overline{B0}$	C_{n+4}	All $\overline{A}$'s, M, C_n	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$	ADD
C_n	to SUM_{OUT}	C_n	Any $\overline{F}$	All $\overline{A}$'s, M	All $\overline{B}$'s	ADD
C_n	to C_{n+4}	C_n	C_{n+4}	All $\overline{A}$'s, M	All $\overline{B}$'s	ADD
SUM_{IN}	to A=B	$\overline{B0}$	A=B	All As, B1, B2, B3, M	C_n	SUBSTRACT
SUM_{IN}	to SUM_{OUT} (Logic Mode)	All $\overline{B}$'s	Any $\overline{F}$	All A's, C_n	M	EXCLUSIVE OR

* ADD Mode: S0, S3 = V_{DD}; S1, S2 = V_{SS}. SUBSTRACT Mode: S0, S3 = V_{SS}; S1, S2 = V_{DD}.

PRESETTABLE UP/DOWN COUNTERS (DUAL CLOCK WITH RESET) 40192-BCD TYPE 40193-BINARY TYPE

GENERAL DESCRIPTION

The MMC 40192, MMC 40193 are monolithic integrated circuits processed in standard Al-gate technology. The MMC 40192 is a 4-Bit Synchronous Up/Down Decade Counter and the MMC 40193 is a 4-Bit Synchronous Up/Down Binary Counter. Counting up and counting down is performed by two count inputs (CLOCK UP and CLOCK DOWN respectively), one being held high while the other is clocked. The outputs (Q_1—Q_4) change on the positive-going transition of this clock. These counters feature preset inputs (J_1—J_4) that are enabled when load ($\overline{\text{PRESET ENABLE}}$) is a logical „0" and a clear (RESET) which forces all outputs to „0" when it is at logical „1". The counters also have CARRY and BORROW inputs so that they can be cascaded using no external circuitry.

FEATURES

- Individual clock lines for counting up or counting down
- Synchronous high-speed carry and borrow propagation delays for cascading
- Active low parallel load
- Active high asynchronous reset
- Quiescent current specified at 20 V
- 5 V, 10 V, 15 V parametric ratings

ABSOLUTE MAXIMUM RATINGS

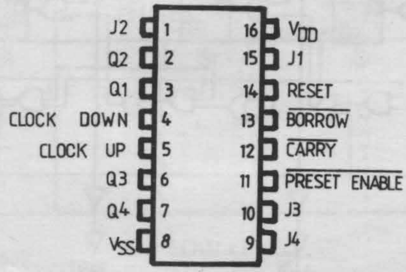
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

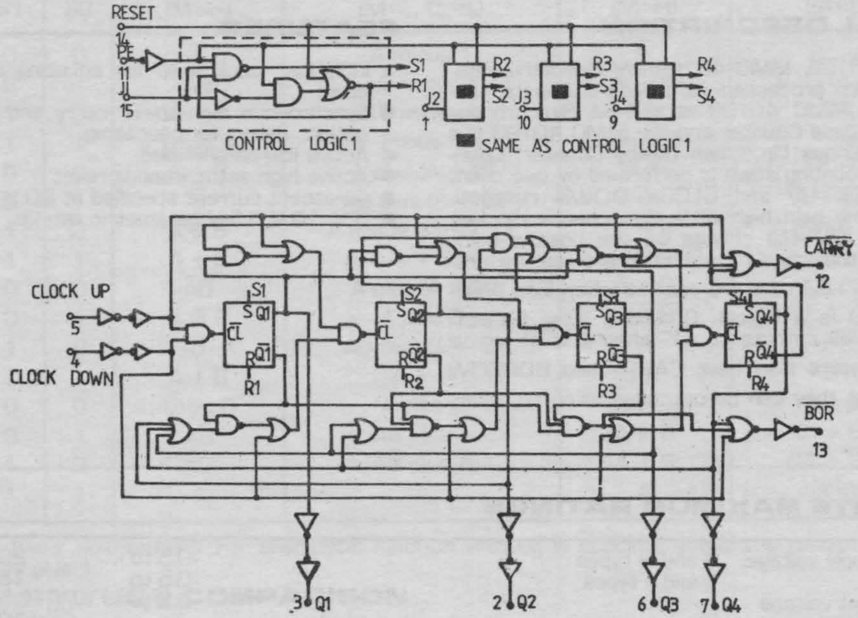
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM

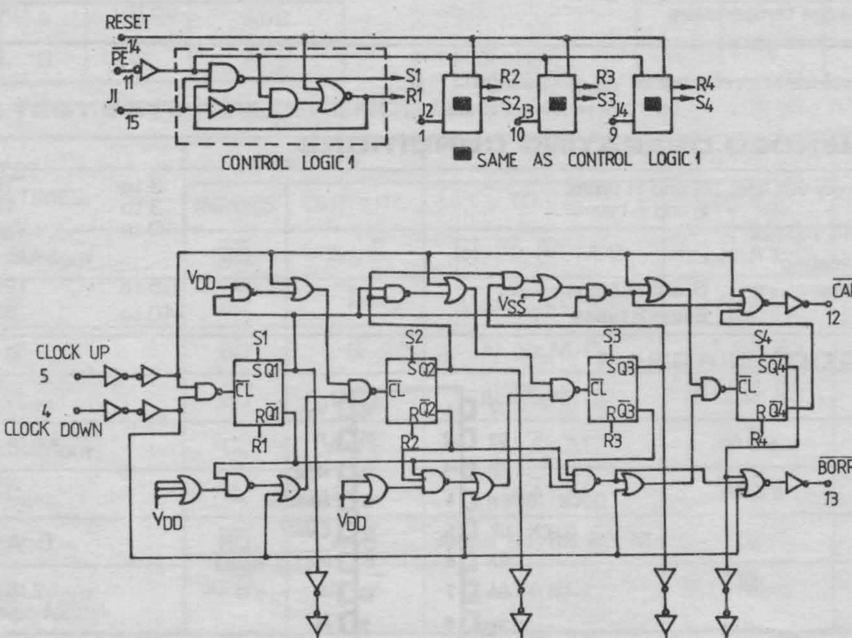


LOGIC DIAGRAM

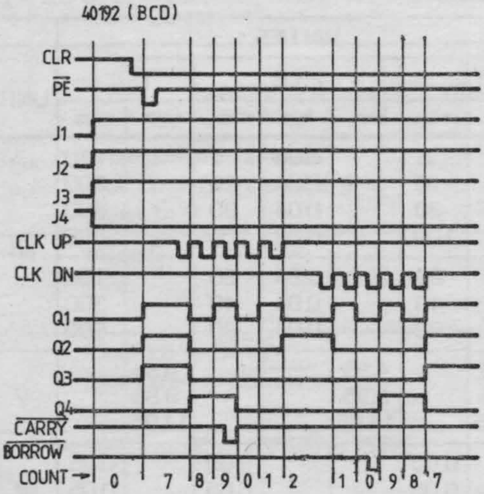
MMC 40192

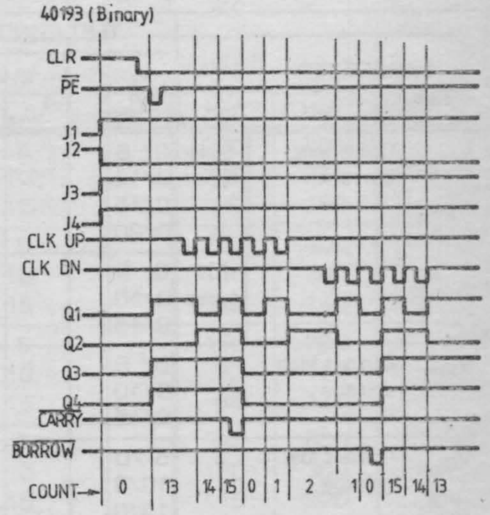


MMC 40193

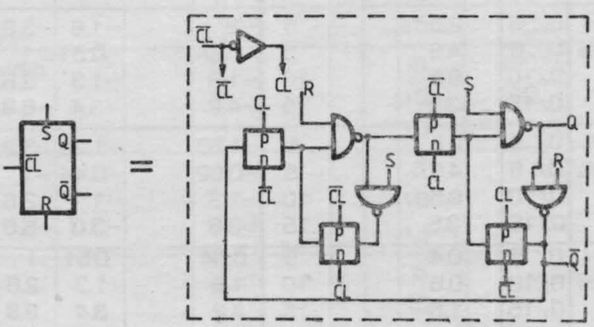


TIMING DIAGRAM





Internal logic of flip-flop



TRUTH TABLE

CLOCK UP	CLOCK DOWN	PRESET ENABLE	RESET	ACTION
	1	1	0	COUNT UP
	1	1	0	NO COUNT
1		1	0	COUNT DOWN
1		1	0	NO COUNT
X	X	0	0	PRESET
X	X	X	1	RESET

1 = HIGH LEVEL 0 = LOW LEVEL X = DON'T CARE

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	VALUES T_{LOW}* min.	T_{LOW}* max.	25°C min.	25°C typ	25°C max.	T_{HIGH}* min.	T_{HIGH}* max.	UNIT
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$\pm10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$\pm10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

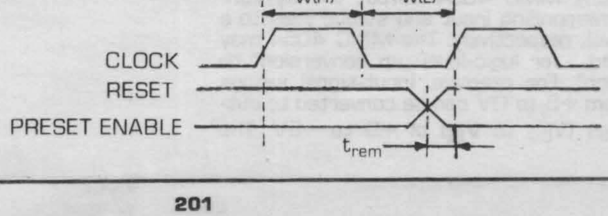
DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

	PARAMETER	TEST CONDITIONS V_{DD}(V)	VALUES min.	typ.	max.	UNIT
t_{PHL}, t_{PLH}	Propagation delay time Clok Up or Clok Down to Q Reset to Q	5		250	500	
		10		120	240	ns
		15		90	180	
	$\overline{PE}$ to Q	5		200	400	
		10		100	200	ns
		15		70	140	
	Clock Up to $\overline{Carry}$ Clok Down to $\overline{Borrow}$	5		160	320	
		10		80	160	ns
		15		60	120	
	$\overline{Reset}$ or $\overline{PE}$ to $\overline{Borrow}$ or $\overline{Carry}$	5		300	600	
		10		150	300	ns
		15		110	220	
t_{THL}, t_{TLH}	Transition time	5		100	200	
		10		50	100	ns
		15		40	80	
t_{rem}*	Removal time Reset or $\overline{PE}$	5	80	40		
		10	40	20		ns
		15	30	15		
t_W	Clock input pulse width Reset	5	480	240		
		10	300	150		ns
		15	260	130		
	$\overline{PE}$	5		120	240	
		10		85	170	ns
		15		70	140	
	Clock	5		90	180	
		10		45	90	ns
		15		30	60	
t_r, t_f	Clock input rise or fall time	5			15	
		10			15	μs
		15			5	
t_{CL}	Maximum clock input frequency	5	2	4		
		10	4	8		MHz
		15	5.5	11		

* The time required for Reset or Preset Enable control to be removed before clocking (see timing diagram).

Timing diagram defining trem



LIQUID-CRYSTAL DISPLAY DRIVERS

4054 - 4 SEGMENT DISPLAY DRIVER-STROBED LATCH FUNCTION
4055 - BCD TO 7-SEGMENT DECODER/ DRIVER, WITH „DISPLAY-FREQUENCY" OUTPUT
4056 - BCD TO 7-SEGMENT DECODER/ DRIVER WITH STROBED LATCH FUNCTION

GENERAL DESCRIPTION

The MMC 4054, MMC 4055, MMC 4056 (G, H types extended temperature range and the E, F types intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in-line plastic or ceramic package. The MMC 4055 and MMC 4056 types are single-digit BCD-to-7-segment decoder/driver circuits that provide level-shifting functions on the chip. This feature permits the BCD input-signal swings (V_{DD} to V_{SS}) to be the same as or different from the 7-segment output-signal swings (V_{DD} to V_{EE}). For example, the BCD input-signals swings (V_{DD} to V_{SS}) may be as low as 0 to −3V, whereas the output-display drive-signal swing (V_{DD} to V_{EE}) may be from 0 to −5V. If V_{DD} to V_{EE} exceeds 15V, V_{DD} to V_{SS} should be at least 4V. The 7-segment outputs are controlled by the DISPLAY-FREQUENCY (DF) input which causes the selected segment outputs to be low, high, or a square-wave output (for liquid-crystal displays).

When the DF input is low the output segments will be high when selected by the BCD inputs. When the DF input is high, the output segments will be low when selected by the BCD inputs. When a square-wave is present at the DF input, the selected segments will have a square-wave output that is 180° out of phase with the DF input. Those segments which are not selected will have a square-wave output that is in phase with the input. DF square-wave repetition rates for liquid-crystal displays usually range from 30 Hz (well above flicker rate) to 200 Hz (well bellow the upper limit of the liquid crystal frequency response). The MMC 4055 provides a level-shifted high-amplitude DF output which is required for driving the common electrode in liquid-crystal displays. The MMC 4056 provides a strobed latchfunction at the BCD inputs. Decoding of all input combinations on the MMC 4055 and MMC 4056 provides displays of 0 to 9 as well as L,P,H,A — and a blank position. The MMC 4054 provides level shifting similar to the MMC 4055 and MMC 4056 independently strobed latches, and common DF control on 4 signal lines. The MMC 4054 is intended to provide drive-signal compatibility with the MMC 4055 and MMC 4056 7-segment decoder types for the decimal point, colon, polarity, and similar display lines. A level-shifted high-amplitude DF output can be obtained from any MMC 4054 output line by connecting the corresponding input and strobe lines to a low and high level, respectively. The MMC 4054 may also be utilized for logic-level „up conversion" or „down conversion". For example, input-signal swings (V_{DD} to V_{SS}) from +5 to 0V can be converted to output-signal swings (V_{DD} to V_{EE}) of +5 to −5V. The level shifted function on all three types permits the use of different input-and output-signal swings. The input swings from a low level of V_{SS} to a high level of V_{DD} while the output swings from a low level of V_{EE} to the same high level of V_{DD}. Thus, the input and output swings can be selected independently of each other over a 3-to 18V range. V_{SS} may be connected to V_{EE} when no level-shift function is required. For the MMC 4054 and the MMC 4056, data are transfered from input to output by placing a high voltage level at the strobe input. A low voltage level at the strobe input latches the data input and the corresponding output segments remain selected (or non-selected) while the strobe is low. Whenever the level-shifting function is required, the MMC 4055 can be used by itself to drive a liquid-crystal display. The MMC 4056, however, must be used together with a MMC 4054 to provide the common DF output.

FEATURES

- Operation of liquid crystals with CMOS circuits provides ultra low-power displays
- Equivalent AC output drive for liquid-cristal displays-no external capacitor required
- Voltage doubling across display (V_{DD} — V_{EE}) = 18V results in effective 36 V (pp) drive across selected display segments
- Low-or high-output level DC drive for other types of displays
- On chip logic-level conversion for different input and output-level swings
- Full decoding of all input combinations: "0-9,L,H,P, A" and blank positions
- Input current of 100 nA at 18V and 25°C for MMC device G, H types
- 100% tested for quiescent current

ABSOLUTE MAXIMUM RATINGS

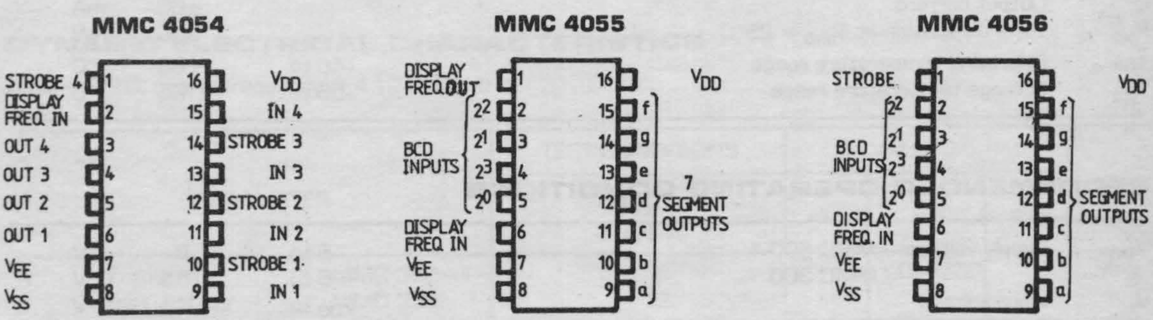
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



MOTOR DRIVE CLOCK CIRCUIT

GENERAL DESCRIPTION

The MMC 300 is a 23 stage binary counter in standard Al-gate CMOS technology in a single monolithic chip. An inverter is available for crystal oscillator application. The function of the trimmer capacitor has been taken over by the variable frequency divider comprised in the IC. Seven adjustment terminals are used to set the divider ratio to the required value with an accuracy of 10^{-6}. The maximum output frequency is set when all adjustment terminals are either open- circuit or connected to pin 14.. If one or more adjustment terminals are grounded (taken to pin 13) the output frequency decreases. The oscillator frequency divided by four may be checked at the test output (pin 8). With an oscillator frequency of 4.194812 MHz the series-connected push-pull output stage supplies a symmetrical square wave signal with a pulse duty factor of 0.5 and a repetition frequency of 0.5 Hz if the variable frequency divider is set to its medium value.
The MMC 300 is available in 14 lead dual in-line and ceramic plastic package.

FEATURES

- Low quiescent power dissipation
- Fully protected inputs
- Adjustable frequency divider in 127 steps
- Test output available

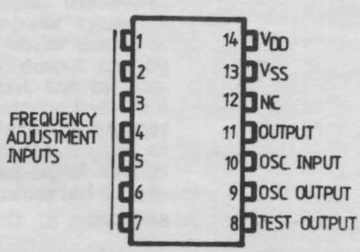
ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage MMC 300—1	−0.3 to	+10	V
	MMC 300	−0.3 to	+17	V
I_{II}	Output current		±60	mA
P_{tot}	Total dissipation at $T_{amb} = 25°C$		200	mW
T_{op}	Operating temperature range	-40 to	+85	°C
T_{stg}	Storage temperature range	-55 to	+125	°C

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: MMC 300-1	5 to	9	V
	MMC 300	6 to	16.5	V
V_i	Input voltage	V_{DD} to	V_{SS}	V
I_{II}	Output current		40	mA
T_{op}	Operating temperature	-40 to	+85	°C

CONNECTION DIAGRAM



3

STATIC ELECTRICAL CHARACTERISTICS

PARAMETER			TEST CONDITIONS V_o (V)	V_{DD} (V)	VALUES 25°C min.	typ.	max.	UNIT
V_{OH}	Output high voltage	MMC 300—1	$I_{OH} = 0$	6	5.99	6		V
		MMC 300		12	11.99	12		V
V_{OL}	Output low voltage	MMC 300—1	$I_{OL} = 0$	6		0	0.01	V
		MMC 300		12		0	0.01	V
I_{DN}	Output Drive current N—channel	MMC 300—1	2	6	20	25		mA
		MMC 300	2	12	33	40		mA
I_{DP}	Output drive current P—channel	MMC 300—1	4	6	20	25		mA
		MMC 300	10	12	33	40		mA
I_{ON}	Current consumption	MMC 300—1		6		3		mA
		MMC 300		12		3		mA
			$I_O = 0$, at quartz frequency of 4. 194812 MHz					

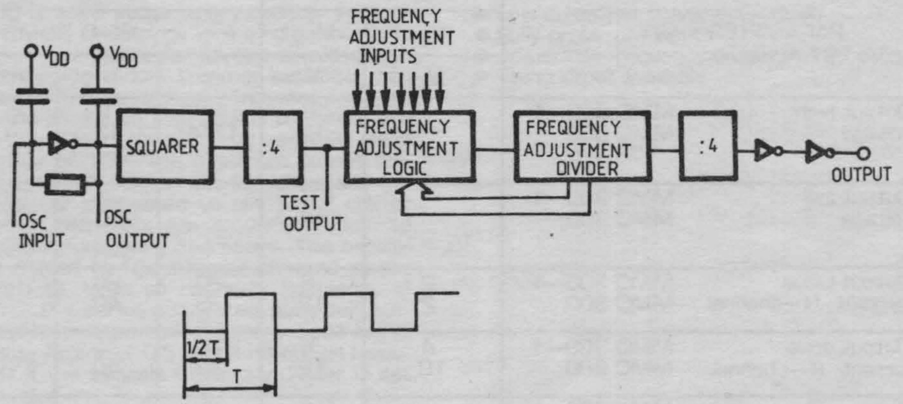
DYNAMIC ELECTRICAL CHARACTERISTICS

($T_{amb} = 25°C$, quartz frequency = 4.194812 MHz)

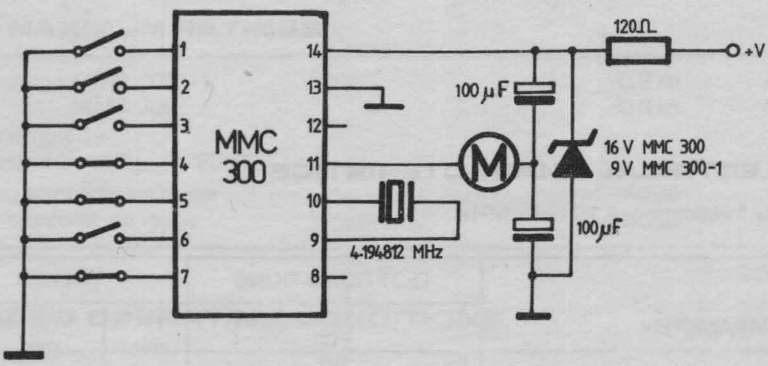
PARAMETER			TEST CONDITIONS V_{DD} (V)	VALUES min.	typ.	max.	UNIT
f_T	Frequency test output	MMC 300—1	6		1.048703		MHz
		MMC 300	12				
f_o*	Output frequency	MMC 300—1	6		0.5		Hz
		MMC 300	12		0.5		Hz
$\frac{\Delta f_o}{f_o}$	Range output frequency adjustment				±121		ppm
R_o	Output resistance		$R_L = 300$			100	Ω

* At the centre position of the variable divider

BLOCK DIAGRAM



TYPICAL APPLICATIONS



AUTO CLOCK

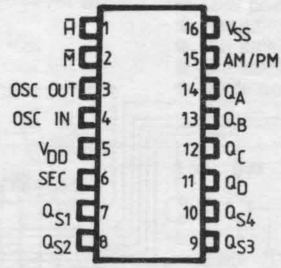
GENERAL DESCRIPTION

The MMC 351 is a metal gate CMOS integrated circuit that provides or controls all signals needed for a $3^1/_2$-digit LED watch. The display format is 12 hours, with an AM/PM indicator. The circuit time base is a 32768 Hz crystal controlled oscillator. The time base frequency is successively divided to provide drive signals for /a multiplexed 7-segment display. In order to drive the display, the watch requires a BCD-to-7 segment decoder (the MMC4511, for example). The device operates from a single 3V to 18V supply. The MMC351 is available in a 16-lead dual-in-line package.

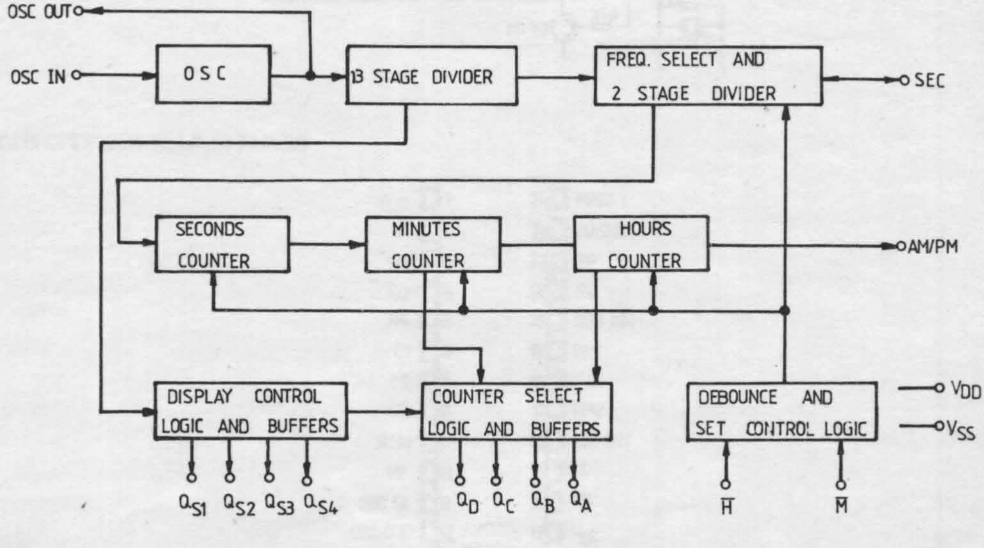
FEATURES

- 32768 Hz crystal controlled oscillator
- wide supply voltage range: 3 to 18V
- low current consumption (3mA)
- 12 hours display format
- on-chip oscillator

CONNECTION DIAGRAM



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

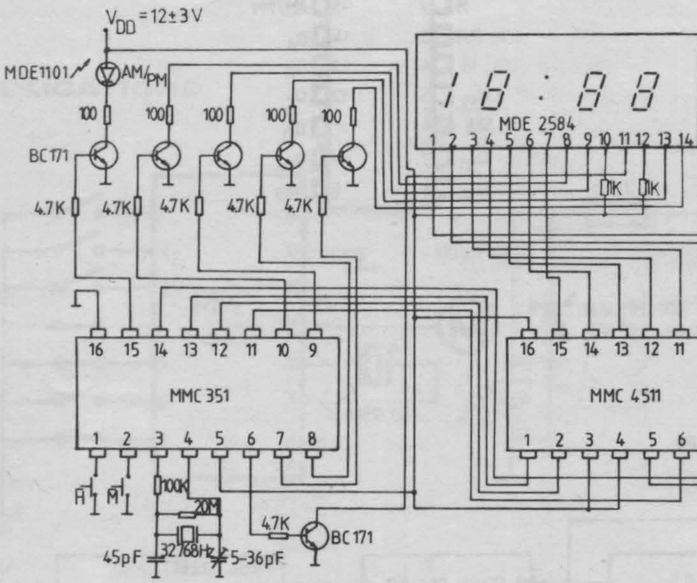
Time base:
The time base of the watch is provided by connecting a crystal controlled RC network to the on-chip CMOS inverter/amplifier.

Display multiplexing:
Outputs from each counter are time-division multiplexed to provide digit-sequential acces to the time data. The $3^1/_2$ digits of the display are multiplexed with a 22% duty cycle, 1024 Hz signal.

Time display:
The hour information is displayed in digit positions 1 and 2, while minute information in digit positions 3 and 4. There are an AM/PM indicator and a seconds serially output.

Time setting:
Closure of the 'M' switch will advance minutes at a 2 Hz rate, with no advance of the hours counter and with seconds counter in 00. Closure of the 'H' switch will advance hours counter at a 1 Hz rate. When POWER ON, minutes counter must be set first.

TYPICAL APPLICATIONS



LOOP DISCONNECT DIALLER

GENERAL DESCRIPTION

The MMC 760 Loop Disconnect Dialler provides the features to implement a pulse dialler with redial. It can be operated directly by the telephone line current and converts a single per key contact into the corresponding pulse signals to simulate the rotary dialler.
When in stand-by condition it requires only few microamperes to maintain the storage of the last call. Keyboard inputs are fully static; outputs are provided to pulse the telephone line and to mute the receiver during impulsing.
Other features are: pin selectable long distance call inhibition, 24 digit memory in wich can be introduced a maximum of 8 access pauses, pin selectable redial inhibition and out pulsing inhibition for operation with payment-card telephones.
Redial can be achieved with two pin selectable procedures.

The device requires an inexpensive 455 kHz ceramic resonator and is designed to minimize external components.
The unique design of the power-on reset circuit can avoid the need for a special dedicated spring in the hook switch.
The loop is disconnected for a time longer than 300 ms when fraudulent dialling is tried with the hook or any external device by sensing the line condition at the input LS.
The MMC 760 is realized in low voltage CMOS technology and can be easily mask programmed to meet all administration standards.

FEATURES

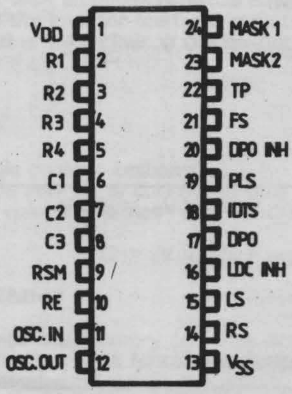
- Direct telephone line operation
- Low voltage CMOS technology
- Low power consumption in stand-by m.
- Pin selectable long distance call inhibition
- Pin selectable output pulsing inhibition
- 8 Selectable access pauses
- Wide selection of mask options for 1,5 — 1,6 — 1,66 — 2 B/W ratios

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	5	V
V_i	Input voltage	V_{SS}−0.5 to V_{DD}+0.5	V
P_{tot}	Total power dissipation	400	mW
T_A	Operating temperature range	−25 to +50	°C
T_{stg}	Storage temperature range	−65 to +85	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
** All voltages are reffered to V_{SS} pin voltage.

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

($T_A = -25°C$ to $+50°C$)

		PARAMETER	TEST CONDITIONS	min.	typ.	max.	UNIT
Supply	V_{DD}	Supply voltage		2.2	2.5	5	V
Supply	I_{DD}	Operating supply current	$V_{DD} = 2.5$ V $f_o = 455$ kHz			0.5	mA
Supply	I_{DD} stand-by	Stand-by supply current (oscillator, off, no external load connected)	$V_{DD} = 2.5$ V			25	µA
Keyboard inputs	Row inputs						
Keyboard inputs	In_H	Input high current	$V_{DD} = 2.5$ V		60	80	µA
Keyboard inputs	In_L	Input low current	$V_{IH} = 2.5$ V			−1	µA
Keyboard inputs	V_{IH}	Input threshold voltage	$V_{IL} = 0$ V	1			V
Keyboard inputs	Column inputs						
Keyboard inputs	I_{IH}	Input high current	$V_{DD} = 2.5$ V			1	µA
Keyboard inputs	I_{IL}	Input low current	$V_{IH} = 2.5$ V		−60	−80	µA
Keyboard inputs	V_{IL}	Input threshold voltage	$V_{IL} = 0$ V			V_{DD}−1 V	V
Oscillator	OSC IN						
Oscillator	I_H	Input high current	$V_{DD} = 2.5$ V, $V_{IH} = 2.5$ V			1	µA
Oscillator	I_L	Input low current	$V_{IL} = 0$ V			−1	µA
Oscillator	OSC OUT						
Oscillator	I_{OH}	Output drive current	$V_{DD} = 2.5$ V, $V_{OH} = 2$ V	−150			µA
Oscillator	I_{OL}	Output sink current	$V_{DD} = 2.5$ V, $V_{OL} = 0.5$ V	150			µA
Mask output	I_{OH}	Output drive current	$V_{DD} = 2.5$ V, $V_{OH} = 1.4$ V	−1			mA
Mask output	I_{OL}	Output sink current	$V_{DD} = 2.2$ V, $V_{OL} = 0.1$ V		20		µA
DPO	I_{OL}	Output sink current	$V_{DD} = 2.2$ V, $V_{OL} = 0.4$ V	1			mA
DPO	I_{OFF}	Output leakage current	$V_{DD} = 2.5$ V			+1	µA
LDC INH, DPO INH, PLS, RSM, RE	I_{IH}	Input high current	$V_{DD} = 2.5$ V, $V_{IH} = 2.5$ V			1	µA
LDC INH, DPO INH, PLS, RSM, RE	I_{IL}	Input low current	$V_{DD} = 2.5$ V, $V_{IL} = 0$ V			−1	µA
LDC INH, DPO INH, PLS, RSM, RE	V_{IH}	Input high voltage		0.7 V_{DD}			V
LDC INH, DPO INH, PLS, RSM, RE	V_{IL}	Input low voltage				0.3 V_{DD}	V
LS	I_{IH}	Input high current	$V_{DD} = 2.5$ V $V_{IH} = 2.5$ V			1	µA
LS	I_{IL}	Input low current	$V_{DD} = 2.5$ V $V_{IL} = 0$ V	−100	−160	−250	µA
LS	V_{IH}	Input high voltage		0.7 V_{DD}			V
LS	V_{IL}	Input low voltage				0.3 V_{DD}	V

		PARAMETER	TEST CONDITIONS	min.	typ.	max.	UNIT
RS	I_{OH}	Output drive current	$V_{DD} = 2.5\ V, V_{OH} = 1.8\ V$	−20			μA
	I_{OL}	Output leakage current				1	μA
	V_{IH}	Input high voltage		0.8 V_{DD}			V
	V_{IL}	Input low voltage				0.2 V_{DD}	V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = -25°C$ to $+50°C$)

	PARAMETER		TEST CONDITIONS	VALUES			UNIT
				min.	typ.	max.	
t_{ACC}	Key access time after last bounce		for all $f_0 = 455$ kHz $V_{DD} = 2.5$ V		5.5		ms
t_{OSC}	Oscillator start-up time					60	ms
t_{MASK}	Mask 1, Mask 2 pulse duration				20		ms
t_{DM}	Mask 1, Mask 2 delay time with respect to DPO				50		ms
t_{PD}	Pre-digital pause				400		ms
t_{DPO}	DPO period	FS = 0			50		ms
		FS = 1			100		ms
t_B/t_M	Break to make ratio				1.6		
t_{IDT}	Interdigit time	IDTS = 0			800		ms
		IDTS = 1			400		ms
t_{RES}	Minimum line break before reset				150		ms
t_{OTO}	Oscillator turn-off time after clear-down LDC INH = 0				150		ms
	LDC INH = 1				300		ms
$t_{LDC\ INH}$	Line break time when LDC INH 1				300		ms

FUNCTIONAL DESCRIPTION

Oscillator (OS IN-OS OUT)

The oscillator has been designed to work with an inexpensive ceramic resonator ($f_0 = 455$ kHz); it requires two external load capacitors (100 pF) and the inverter feedback resistor.
The oscillator starts after LS (line sense) is taken low; it comes back to the stand-by mode after LS has gone high for at least 150 ms (or 300 ms if LDC-INH high).

Keyboard (R_1 to R_4, C_1 to C_3)

MMC 760 is designed to work with a single contact keyboard.
A valid key entry is recorded when a single row pin is connected to a single column pin. All the input combinations except a single row and a single column are not recognized. A valid key is entered after 5ms from the last key bounce.

Outpulsing inhibition (DPO INH)

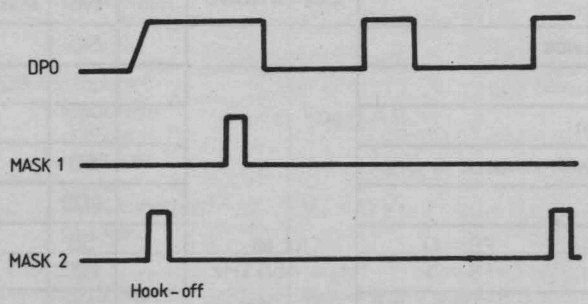
If this pin is low, digits can be entered into the memory but they are not sent on the line: when DPOINH goes high the stored digits are sent on the line. This function is realized to allow operations with payment-card telephones in which it is sometimes needed to assess the validity of the payment-card.

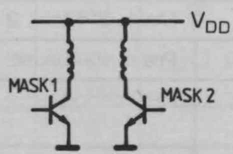
Dial pulse output (DPO)

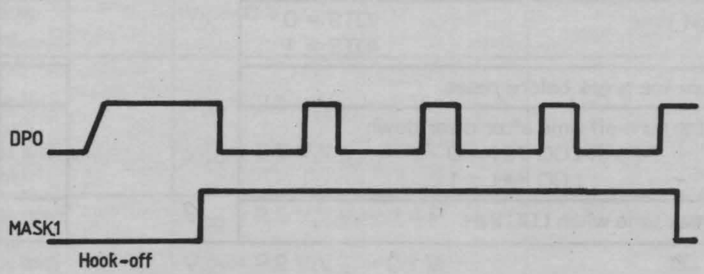
When a valid key is recognized the line must be opened and closed at a fixed rate and the total number of break pulses corresponds to the number of the selected key (10 line breaks are associated to the key „0"). DPO is an open drain output; line breaks occur when DPO is active to ground.

Mask Outputs (MASK 1, MASK 2)

The Mask outputs are used to mute the speech circuit during signalling. In telephones using conventional speech circuits muting is generally achieved by short-circuiting with a two-winding, bistable reed-relay. In this case MASK 1 and MASK 2 provide pulse outputs to drive the winding which close and open the contact respectively.
In telephones with electronic speech circuits muting is implemented electronically. In this case a metal option transforms MASK 1 into a signal which remains high throughout signalling.







Redial enable (RE)

Redial of the last call is possible according to the procedures described below only if RE is high. Redial is never allowed when RE is low.

Redial Selection Mode (RSM)

The last number redialling facility operates in two modes. In the first (RSM high) the key sequence** 0 will repeat the last number dialled. The last number memory can be cleared by the # key. In the second case (RSM low) the last number dialled is only stored if the key* is pressed before replacing the handset. As before, the sequence** 0 starts the last number repeat. In both cases the stored number is unaffected by incoming calls. The redial request can be simplified by a mask option to the single key*, instead of the sequence** 0.

Pause length selection (PLS)

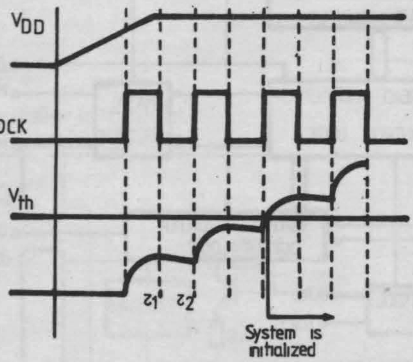
Interdigit pauses are available to interrupt outpulsing to give to the exchange the possibility of switching from a private to a public line. The device memorizes automatically a pause when the first digit is zero; a maximum of 7 pauses can be added during dialling by selecting key*. These pauses are active only during readialling and have a duration of 3 sec if PLS is low or 20 sec if PLS is high; in both cases pause duration can be shortened pushing key*.

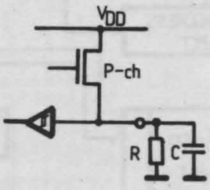
Line sense (LS)

This input senses if the line loop is closed or not
LS = high means loop open
LS = low means loop closed
When LS is kept high for more than 150 ms the circuit is reset (if LDCINH = 0). When LDCINH = 1 reset occurs after 300 ms.

Reset (RS)

This input/output pin is used to turn off the oscillator when line interrupts of more than 150 ms are sensed; it is also used as a power-on reset in applications where redial is not allowed. When the hand-set is picked-up and V_{DD} increases over its minimum value, the oscillator starts and an external capacitor is charged above a fixed threshold level by an opendrain P-ch. transistor driven by a 150 kHz clock. Reset occurs after a line interrupt of more than 150 ms; the pull-up transistor goes off and the capacitor discharges through a resistor to GND level.





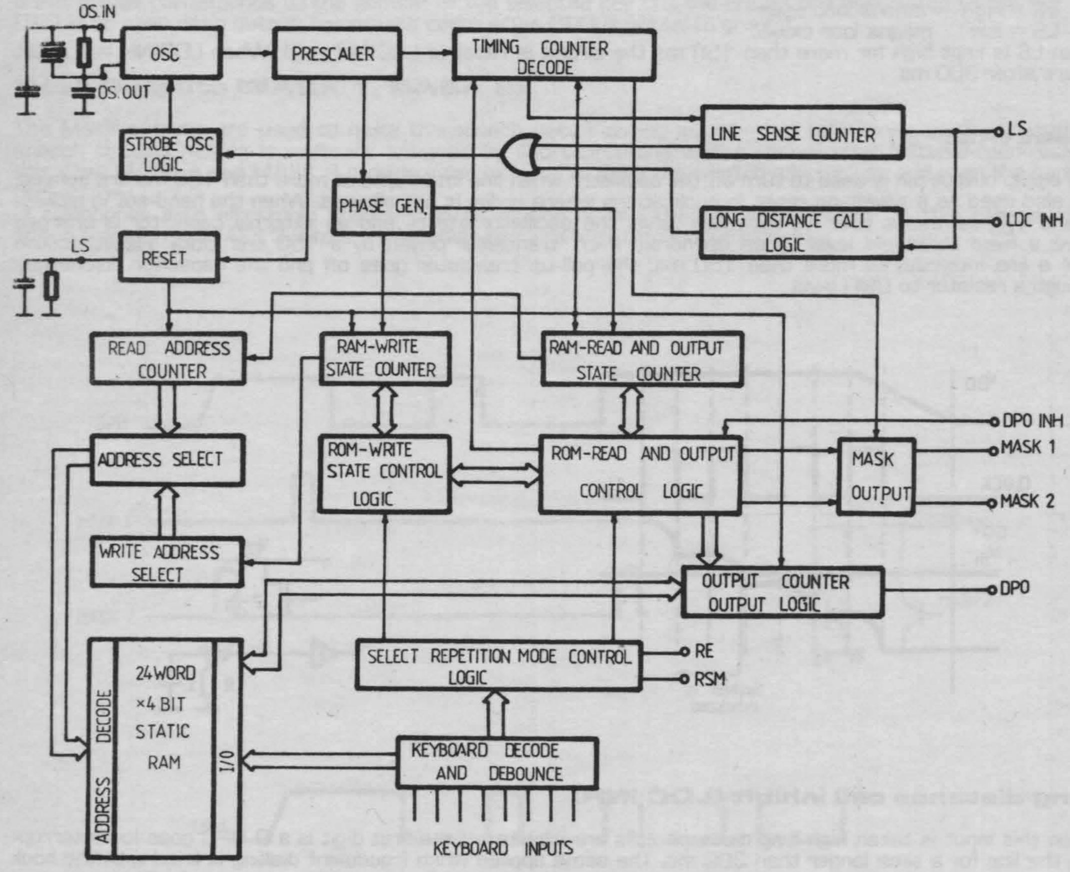
Long distance call inhibit (LDC INH)

When this input is taken high long distance calls are inhibited; if the first digit is a 0 DPO goes low interrupting the line for a time longer than 300 ms. The same applied when fraudulent dialling is tried with the hook or any external device by sensing the line condition at the input LS. When INH is low this facility is inoperative.

Test pin (TP)

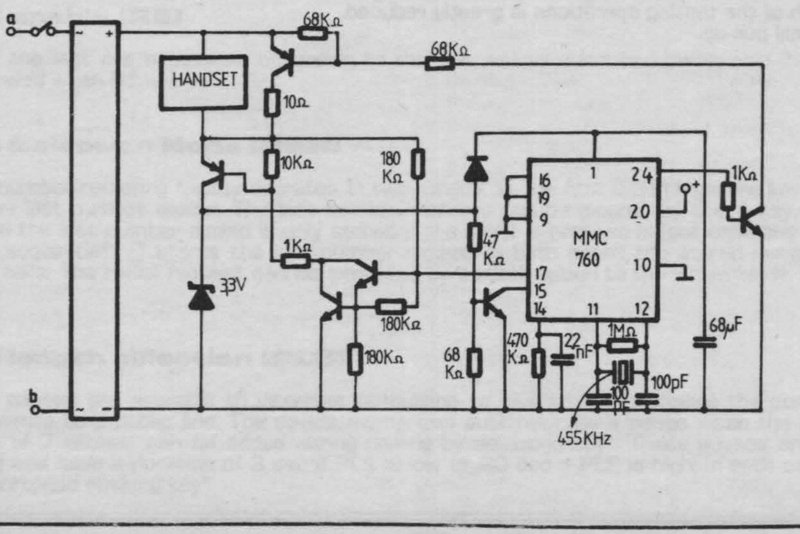
When this input is taken low all the timing values are divided by 100.
In this way the length of the testing operations is greatly reduced.
This pin has an internal pull-up.

BLOCK DIAGRAM

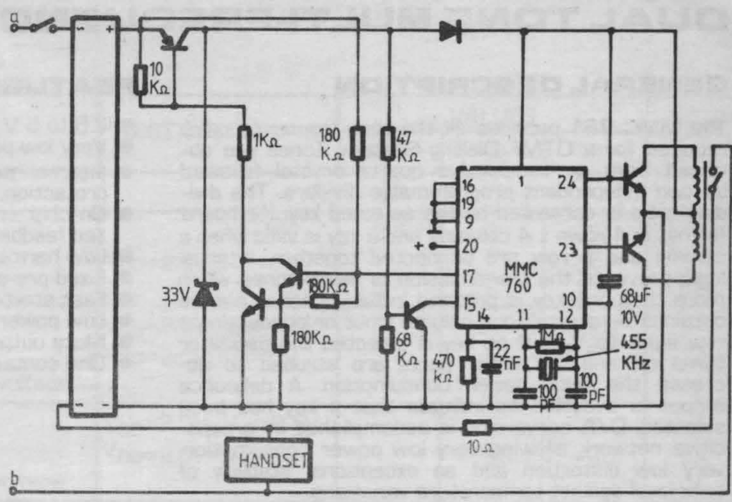


TYPICAL APPLICATIONS

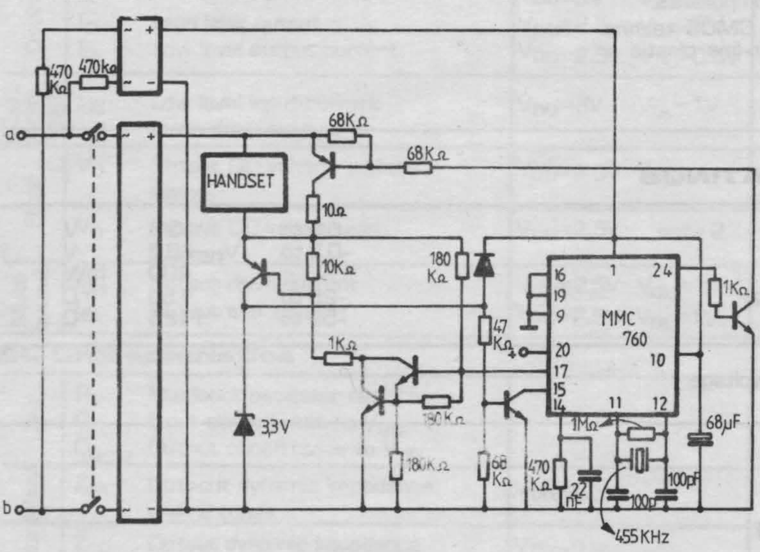
Typical serial applications



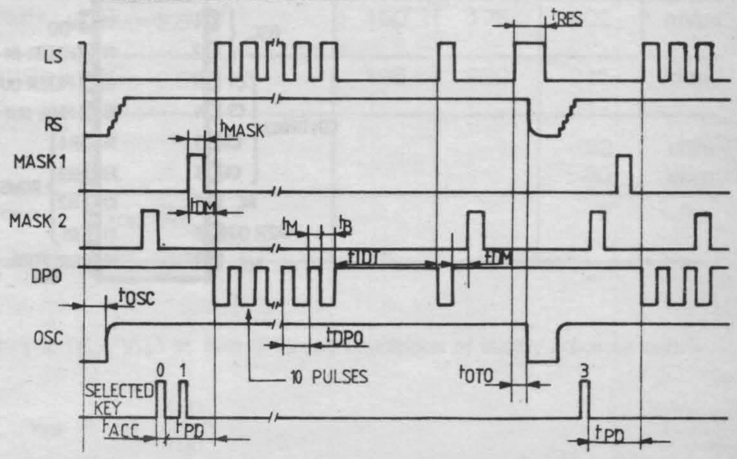
With bistable relay



Pulse dialler with redial



TIMING DIAGRAM



DUAL TONE MULTI-FREQUENCY GENERATOR

GENERAL DESCRIPTION

The MMC 761 provides all the tone frequency pairs required for a DTMF Dialling System. Tones are obtained from an inexpensive quartz crystal followed by two independent programmable dividers. The dividing ratio is controlled by the selected key. Keyboard format is 4 rows x 4 columns and a key is valid when a column and a row are connected together. Internal logic prevents the transmission of illegal tones when more than one key is pressed Individual tones can be obtained by grounding a column input or connecting a row input to V_{DD}. If no key is selected the oscillator turns off and the linear parts are strobed to decrease the total power consumption. A debounce output is available, to indicate that a key has been selected. D/A conversion is accomplished by a capacitive network allowing very low power consumption, very low distortion and an exceptional stability of tone level against temperature variations.

The tones are mixed in a resistive network; a unity gain amplifier is provided to realize a two pole active filter with only four external passive components.

The MMC 761 utilizes low voltage CMOS technology and is available in 18 pin dual-in-line plastic or ceramic package.

FEATURES

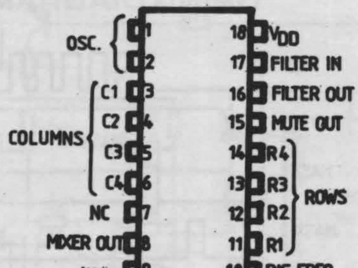
- 2.5 to 5 V supply range.
- Very low power consumption
- Internal pull-up or pull-down resistor with diode protection on all keyboard inputs
- On-chip crystal controlled oscillator with integrated feedback resistor and load capacitors
- Low harmonic distortion
- Fixed pre-emphasis on high-group tones
- Fast start-up time
- Low power consumption in stand-by mode
- Mute output
- One contact per key

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	-0.5 to	+5.5	V
V_I	Input voltage	-0.3 to	V_{DD}+0.5	V
P_{tot}	Power dissipation		400	mW
T_A	Operating temperature range	-25 to	+50	°C
T_{stg}	Storage temperature range	-55 to	+125	°C

* All voltages are referred to V_{SS} pin voltage

CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS

(All parameters are tested at $T_A = 25°C$)

		PARAMETER	TEST CONDITIONS	VALUES min.	VALUES typ.	VALUES max.	UNIT
DC Characteristics							
Supply	V_{DD}	Voltage supply voltage		2.5	3	5	V
Supply	I_{DD}	Operating supply current	V_{DD}=2.5V			2	mA
Supply	I_{DDO}	Stand-by supply current				0.5	mA
Row inputs	I_{IH}	High level input current	V_{DD}=2.5V V_{IH}=2.5V		60	80	µA
Row inputs	I_{IL}	Low level input current	V_{DD}=2.5V V_{IL}=0V			1	µA
Row inputs	V_{IH}	High level input threshold voltage		1			V
Column inputs	I_{IH}	High level input current	V_{DD}=2.5V V_{IN}=2.5V			1	µA
Column inputs	I_{IL}	Low level input current	V_{DD}=2.5V V_{IL}=0V		−60	−80	µA
Column inputs	V_{IL}	Low level input threshold voltage				V_{DD}−1V	V
Oscillator	I_{IH}	High level input current	V_{DD}=3V V_{IN}=3V			1	µA
Oscillator	I_{IL}	Low level input current	V_{DD}=3V V_{IL}=0V			1	µA
Oscillator	I_{OH}	High level output,	V_{DD}=2.5V V_{OH}=2V	−300	−500		µA
Oscillator	I_{OL}	Low level output current	V_{DD}=2.5V V_{OL}=0.5V	300	500		µA
Digit freq. outp.	I_{OL}	Low level input current (open drain output)	V_{DD}=3V V_{OL}=1V	200			µA
Filter	V_O	Output DC voltage without tones	V_{DD}=2.5V			200	mV
Filter	V_O	Output DC voltage with 2 tones	V_{DD}=2.5V note 2.	0.81	0.84	0.87	V
Mute output	I_{OH}	Output drive current	V_{DD}=2.5V V_{OH}=1.5V	100			µA
Mute output	I_{OL}	Output sink current	V_{DD}=2.5V V_{OL}=1V	20			µA
AC Characteristics							
Osc	R_F	Feedback oscillator resistence		4	4.5		MΩ
Osc	C_I	Input capacitance to V_{DD}			9.5	10.5	pF
Osc	C_O	Output capacitance to V_{DD}			10.5	11.5	pF
Mixer	Z_{01}	Outpout dynamic impedance with 2 tones	V_{DD}=2.5V		10		kΩ
Filter	Z_{02}	Output dynamic impedance with 2 tones	V_{DD}=2.5V		2.5		kΩ
charachteristics	V_{LF}	Low frequency tones amplitude at pin 14	V_{DD}=2.5V	150	175	200	mVpp
charachteristics	V_{HF}	High frequency tones amplitude at pin 14	V_{DD}=2.5V	195	220	245	mVpp
charachteristics		Unwanted frequency components at f = 3.4 kHz				−33	dBm
charachteristics		at 50 kHz				−80	dBm
Ton.		Total harmonic distortion for a single frequency	V_{DD}=2.5 V			2	%

Note 1: The value of AC output components (V_{LF}, V_{HF}) at two different conditions of supply voltages can be relates as follows:

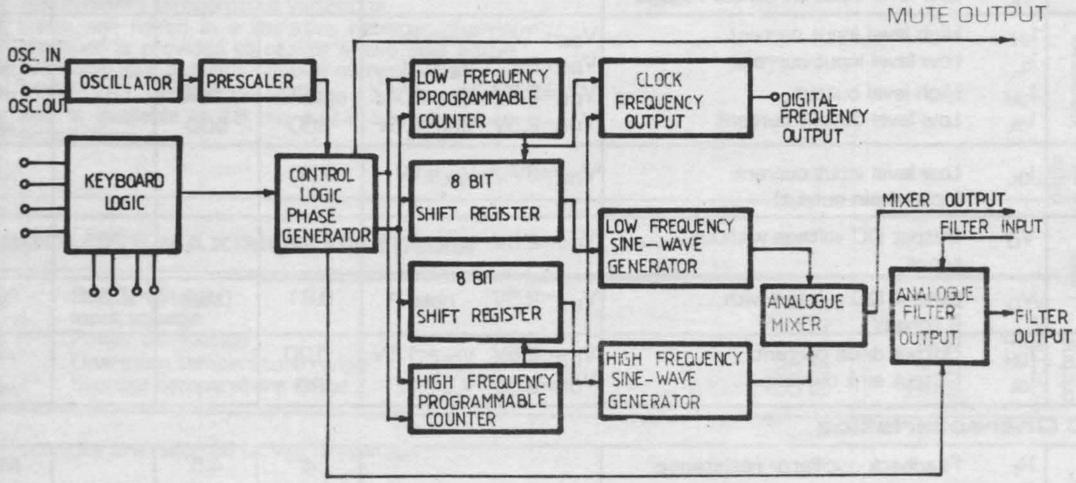
$$V_{LF'} = V_{LF} \frac{V_{DD'}}{V_{DD}} \qquad V_{HF'} = V_{HF} \frac{V_{DD'}}{V_{DD}}$$

	PARAMETER	TEST CONDITIONS	VALUES			UNIT
			min.	typ.	max.	
t_s	Start up time	V_{DD}=2.5 V		3	5	ms
t_r	Supply voltage rise time	V_{DD}=2.5 V			250	ms

Note 1: The value of DC output component at two different condition of supply voltages, with two tones activiated, cau be related as follows.

$$V_{DC'} = V_{DC} \frac{V_{DD'}}{V_{DD}}$$

BLOCK DIAGRAM



CMOS CLOCK GENERATOR

GENERAL DESCRIPTION

The MMC 9500 is a CMOS circuit designed to generate the two phase clok required by the MMP 9100 Push Button Dialler and the repertory dialler circuit. It consists of an RC oscillator, a level shifter, a 2 phase clock generator and driver, and a clocked D-type bistable. The RC oscilator is set by external components to run at 36 kHz and is normally operated from a 4 V supply to minimize power consumption. The oscillator output is shifted and used to drive the two phase clock generator which is normally run on a 14 V supply. The D-type bistable is either used as a reset generator for the MMP 9100, or it is used to drive a voltage multiplier to generate the 14 V supply.

FEATURES

- Generates 2 phase clock from single power supply
- Operates with MMP 9100 Push Button Dialler
- Very low power consumption, allowing use of line powered telephones
- Minimeze external components in push button telephones
- Stable generation of clock frequencies

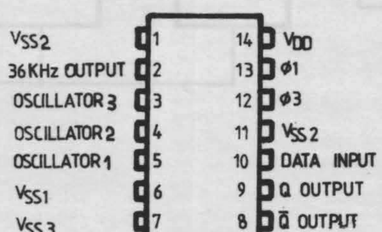
ABSOLUTE MAXIMUM RATINGS

Voltage at any pin with respect to V_{SS}	−18V	to	+0.3 V
Storage temperature T_{stg}	−65°C	to	150°C
Operating temperature T_A	−25°C	to	70°C

RECOMMENDED OPERATING CONDITIONS

$V_{DD} = 0$ V
$V_{SS1} = -4$ to -15 V
$V_{SS2} = -4$ to -15 V
$V_{SS3} = -4$ to -15 V
$f_{clock} = 36$ kHz ±10%
$T_A = +25$°C

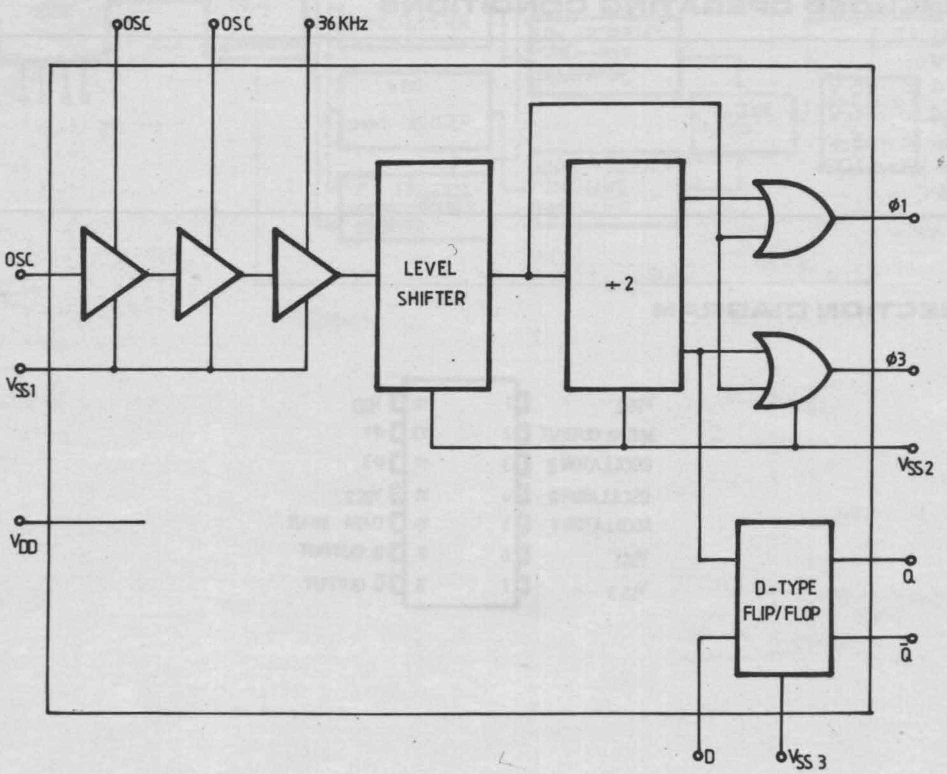
CONNECTION DIAGRAM



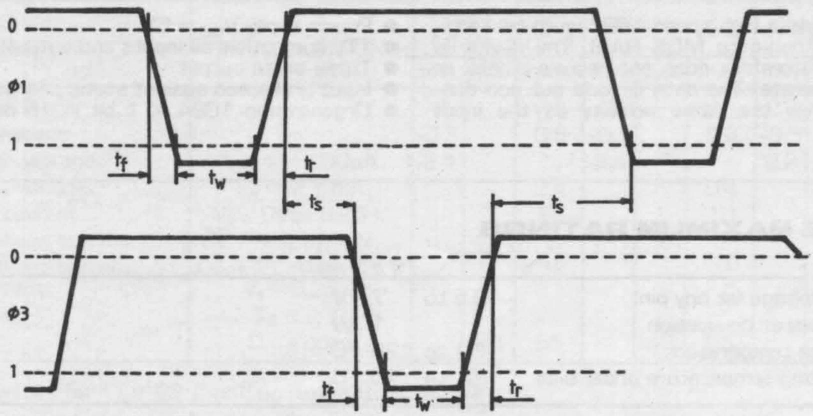
ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES			UNIT
		min.	typ.	max.	
Clock outputs					
t_r rise time	360 pF load	—	90	200	ns
t_f fall time	360 pF load	—	120	250	ns
t_w pulse width	at 36 kHz	10	—	—	μs
t_s pulse separation	at 36 kHz	10	—	—	μs
Stability	with supply and temperature	—	—	±5%	
Output on-resistence					
Ø1, Ø3	VSS2 = −4 V	—	0.3	2	kΩ
Q, $\bar{Q}$	VSS3 = −4 V	—	200	750	Ω
Supply current					
ISS1	VSS1 = −4 V	—	130	200	μA
ISS2	VSS2 = −15 V, 10 pF load	—	100	200	μA
ISS3	VSS3 = −15 V	—	30	50	μA

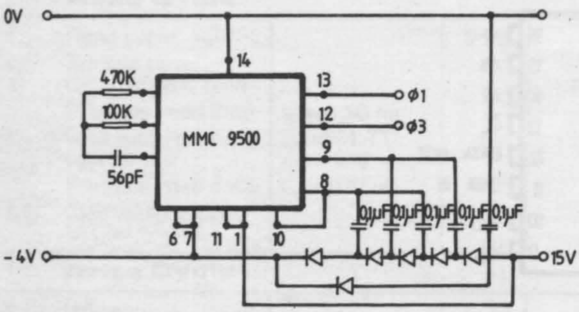
BLOCK DIAGRAM

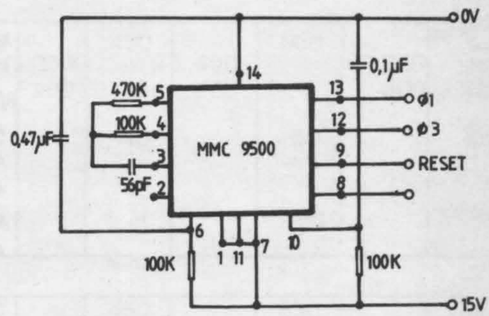


WAVEFORMS



TYPICAL APPLICATIONS





1024 BIT STATIC RANDOM-ACCESS MEMORY

GENERAL DESCRIPTION

The MMN 2102 is a high speed 1024 word by 1 static N-channel silicon-gate MOS RAM. The device is fully static and therefore does not require clocks or refreshing to operate. The data is read out non destructively and has the same polarity as the input data.

FEATURES

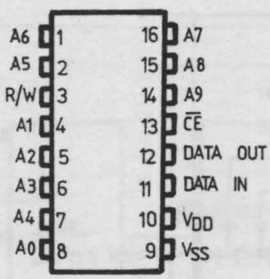
- Power suplly V_{CC} = 5V
- TTL compatible all inputs and outputs
- Three-state output
- Input protected against static charge
- Organization 1024 × 1 bit in 16 pin std. package

ABSOLUTE MAXIMUM RATINGS

V_i	Input voltage (at any pin)	-0.5 to 7	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature	-33 to 125	°C
T_{op}	Operating temperature under bias	0 to 70	°C

All voltages are referred to GND pin voltage

CONNECTION DIAGRAMS



TRUTH TABLE

CE	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	HIGH Z	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_{OUT}	READ

STATIC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.25V, T_A = 0 to 70°C unless otherwise specified)

PARAMETER		TEST CONDITIONS	MMN 2102 MMN 2102-4			MMN 2102-2			MMN 2102-6			UNIT
			min.	typ.	max.	min.	typ.	max.	min.	typ.	max.	
V_{IH}	Input high voltage		2		V_{CC}	2		V_{CC}	2.2		V_{CC}	V
V_{IL}	Input low voltage		-0.5		0.8	-0.5		0.8	-0.5		0.65	V
V_{OH}	Output high voltage	$I_{OH} = -100\mu A$	2.4			2.4			2.2			V
V_{OL}	Output low voltage	$I_{OL} = 2.1$ mA			0.4			0.4			0.45	V
I_{LI}	Input load current	V_I = 0V to 5.25 V		1	10		1	10		1	10	µA
I_{OH}	Output leakage current	$\overline{CE} = 2V$, $V_O = V_{OH}$		1	5		1	5		1	5	µA
I_{OL}	Output leakage current	$\overline{CE} = 2V$, $V_O = 0.4$ V		-1	-10		-1	-10		-1	-10	µA
I_{CC}	Supply current	$V_I = 5.25V$, $T_A = 0°C$ D_{OUT} open		33	55		45	65		33	55	mA

Note: typical values for T_A = 25°C and nominal supply voltage

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5 V unless otherwise specified)

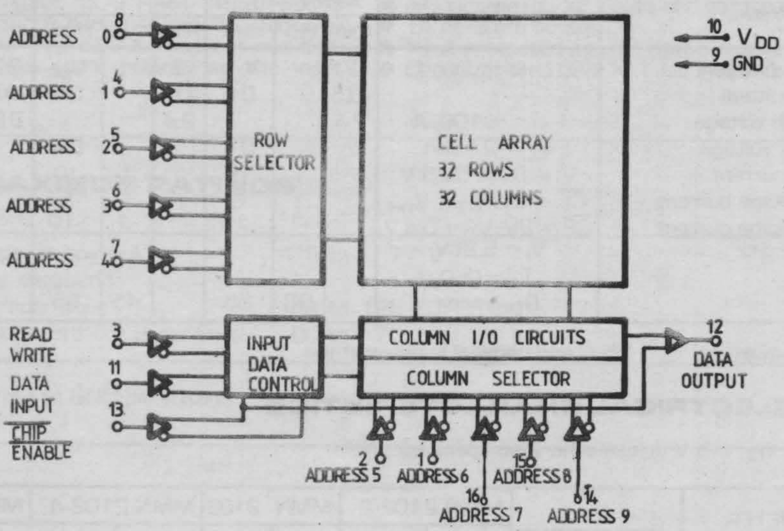
PARAMETER		TEST CONDITIONS	MMN 2102-2		MMN 2102		MMN 2102-4		MMN 2102-6		UNIT
			min.	max.	min.	max.	min.	max.	min.	max.	
	Read Cycle										
t_{rc}	Read cycle		250		350		450		650		ns
t_a	Access time			250		350		450		650	ns
t_E	CE to output time			130		180		230		400	ns
t_{OH1}	Previous read data valid with respect to address	$t_R t_F$ = 10 ns Load = 1 TTL gate and	40		40		40		50		ns
t_{H2}	Previous read data valid with respect to chip enable	C_L = 100 pF	0		0		0		0		ns
	Write Cycle										
t_{WC}	Write cycle		250		350		450		650		ns
t_{AW}	Address to with setup time	$t_R t_F$ = 10 ns	20		20		20		200		ns
t_{WP}	Write pulse width	Load = 1 TTL	180		250		300		400		ns
t_{WR}	Write recovery time	gate and	0		0		0		50		ns
t_s	Data setup time	C_L = 100 pF	180		250		300		450		ns
t_{CW}	Chip enable to write Set up time		180		250		300		550		ns

CAPACITANCE

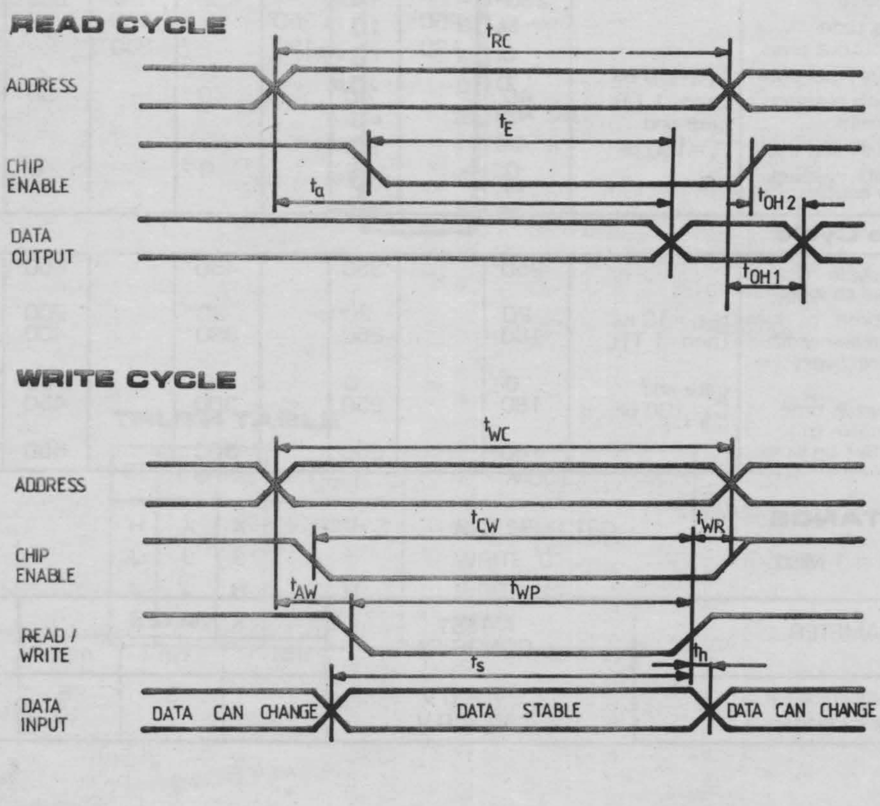
(T_A = 25°C, f = 1 Mhz)

PARAMETER		TEST CONDITIONS	VALUES			UNIT
			min.	typ.	max.	
C_I	Input capacitance	V_I = 0 V		3	5	pF
C_O	Output capacitance	V_O = 0 V		7	10	pF

BLOCK DIAGRAM



WAVEFORMS



1024 × 4 BIT STATIC RAM

GENERAL DESCRIPTION

MMN 2114 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using a high performance MOS technology. It uses fully DC static circuitry throughout, in both array and decoding; therefore it requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data.

Common input/output pins are provided. MMN 2114 is designed for memory applications where high performance and high reliability, low cost, large bit storage, and simple interfacing are important design objectives.

MMN 2114 is placed in an 18-pin package for the highest possible density. It is directly TTL compatible in all respects: inputs, outputs, a single +5 V supply.

A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied.

FEATURES

- single +5 V supply
- identical cycle and access times
- completely static memory — no clock or timing strobe required
- directly TTL compatible: all inputs and outputs
- common data input and output using three-state outputs
- high density 18 pin package

ABSOLUTE MAXIMUM RATINGS

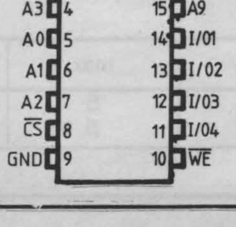
T_A	Temperature under bias	-10°C to	80°C
T_{stg}	Storage Temperature	−65°C to	150°C
V_i	Voltage on any Pin with Respect to ground	−0.5 V to	+7 V
P_{tot}	Power dissipation		1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Exposure to absolute maximum rating conditions for extended periods may affeet device reliability.

PIN CONNECTIONS



PIN NAMES

A0–A9	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
I/01–I/04	DATA INPUT/OUTPUT		

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5 V ± 5% (Unless otherwise specified)

	PARAMETER	TEST CONDITIONS	MMN 2114-2, 2114-3, 2114 min.	max.	UNIT
I_{LI}	Input Load Current (All input pins)	V_{IN} = 0 to 5.25 V		10	μA
$\|I_{LO}\|$	I/O Leakage Current	$\overline{CS}$ = 2.4 V, $V_{I/O}$ = 0.4 V to V_{CC}		10	μA
I_{CC1}	Power Supply Current	V_{CC} = 5.25 V, $I_{I/O}$ = 0 mA, T_A = 25°C		95	mA
I_{CC2}	Power Supply Current	V_{CC} = 5.25 V, $I_{I/O}$ = 0 mA, T_A = 0°C		100	mA
V_{IL}	Input Low Voltage		−0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}	V
I_{OL}	Output Low current	V_{OL} = 0.4 V	2.1	6.0	mA
I_{OH}	Output High current	V_{OH} = 2.4 V	−1.0	−1.4	mA

A.C. CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 5 V ± 5% (Unless Otherwise Specified)

	PARAMETER	2114-2 min.	2114-2 max.	2114-3 min.	2114-3 max.	2114 min.	2114 max.	UNIT
Read cycle								
t_{RC}	Read Cycle Time	200		300		450		ns
t_A	Access Time		200		300		450	ns
t_{CO}	Chip Select to Output Valid		70		100		120	ns
t_{CX}	Chip Select to Output Enabled	20		20		20		ns
t_{OTD}	Chip Deselect to Output Off		60		80		100	ns
t_{OHA}	Output Hold From Address Change	50		50		50		ns
Write cycle								
t_{WC}	Write Cycle Time	200		300		450		ns
t_W	Write Pulse Width	120		150		200		ns
t_{WR}	Write Release Time	0		0		0		ns
t_{OTW}	Write to Output Off		60		80		100	ns
t_{DW}	Data to Write Overlap	120		150		200		ns
t_{DH}	Data Hold	0		0		0		ns

CAPACITANCE

T_A = 25°C, f = 1.0 MHz

	PARAMETER	typ	max	UNIT
$C_{I/O}$	Input/Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note:This parameter is periodically sampled and not 100% tested.

A.C. TEST CONDITIONS

Input Pulse Levels		0.8 V to 2V
Input Rise and Fall Time		10 ns
Timing Measurement Levels:	Input	1.5 V
	Output	0.8 V and 2V
Output Load		1 TTL Gate and 100 pF

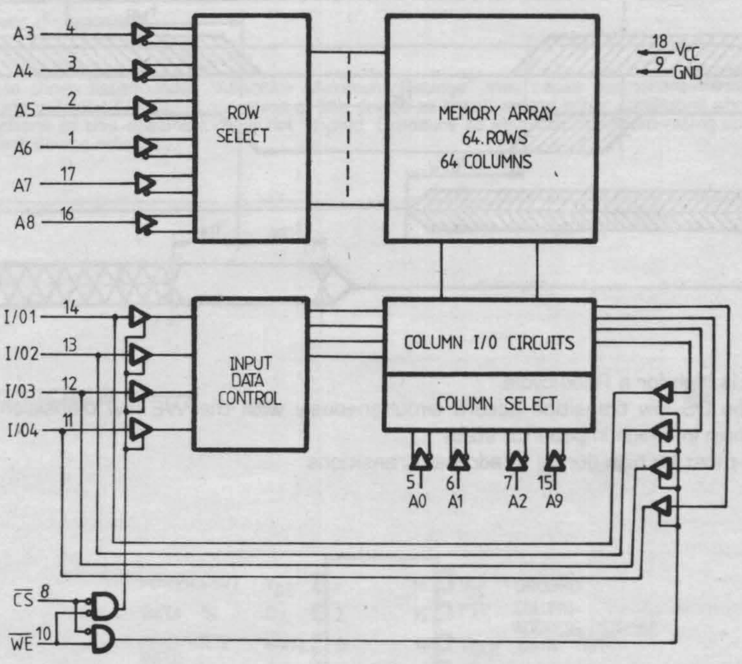
DATE STORAGE

When $\overline{WE}$ is high, the data input buffers are inhibited to prevent erroneous data from being written into the array. As long as $\overline{WE}$ remains high, the data stored cannot be afected by the Address, Chip Select, or Data I/O logic levels or timing transitions.

Data storage also cannot be affected by $\overline{WE}$, Addresses, or the I/O ports as long as CS is high. Either CS or $\overline{WE}$ or both can prevent extraneous writing due to signal transitions.

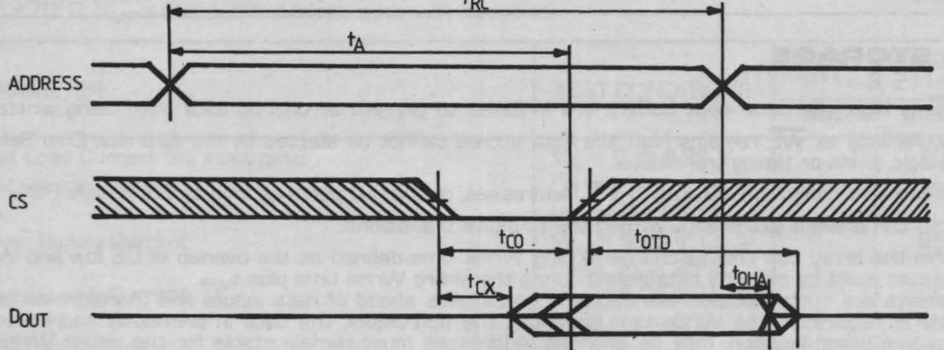
Data within the array can only be changed during Write time-defined as the overlap of $\overline{CS}$ low and $\overline{WE}$ low. The addresses must be properly established during the entire Write time plus t_{WR}.
Internal delays are such that address decoding propagates ahead of data inputs and therefore no address setup time is required. If the Write time precedes the addresses, the data in previously addressed locations, or some other location, may be changed. Addresses must remain stable for the entire Write cycle but the Data Inputs may change. The data which is stable for t_{DW} at the end of the Write time will be written into the addressed location.

BLOCK DIAGRAM

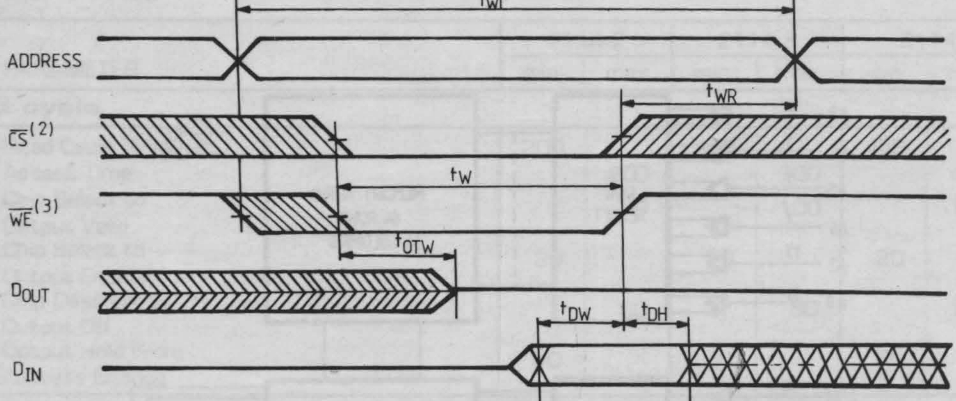


WAVEFORMS

Read cycle (1)



Write cycle



Notes: 1. $\overline{WE}$ is high for a Read cycle.
2. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition, the output buffers remain in a high impedance state
3. $\overline{WE}$ must be high during all address transitions

4096 - BIT DYNAMIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION

The MMN 4027 is a 4096 word by 1 bit dynamic N-channel silicon gate MOS RAM. The MMN 4027 uses a single transistor cell utilizing a dynamic storage technique and dynamic control circuitry with low power dissipation. A unique multiplexing and latching technique for the address inputs permits the MMN 4027 to be mounted in a standard 16-pin package. The MMN 4027 incorporates several flexible operating modes. In addition to the usual read and write cycles, read modify write, page mode and RAS-only refresh cycles are available with the MMN 4027. Page mode timing is very useful in systems requiring Direct Memory Access (DMA). The device is available in 16-lead dual in-line plastic or ceramic package (metal-seal), and ceramic package (frit-seal).

FEATURES

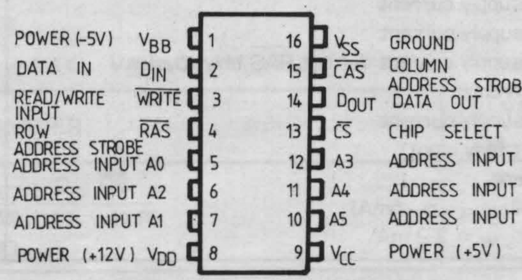
- Power supply V_{DD} = 12 V, V_{CC} = 5 V, V_{BB} = -5 V (all with ± 10% tolerance)
- All inputs are low capacitance and TTL compatible
- Input latches for addresses, chip select and data in
- Inputs protected against static charge
- Three-state TTL compatible output
- Output data latched and valid into next cycle
- ECL compatible on V_{BB} power supply (-5.7 V.)
- Low power consumption :
  - active power under 470 mW
  - standby power under 27 mW

ABSOLUTE MAXIMUM RATINGS*

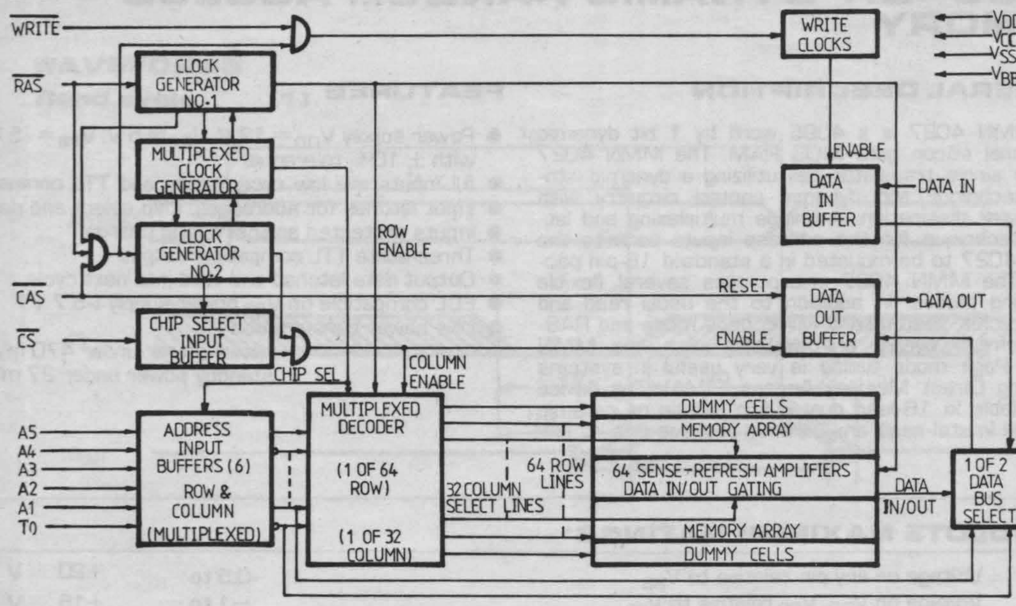
	Voltage on any pin relative to V_{BB}	-0.5 to	+20	V
	Voltage on V_{DD}, V_{CC} relative to V_{SS}	−1 to	+15	V
	$V_{BB} - V_{SS}$ ($V_{DD} - V_{SS} > 0$)		0	V
T_A	Operating temperature	0 to	+70	°C
T_{stg}	Storage temperature for ceramic package	-65 to	+150	°C
	for plastic package	-55 to	+125	°C
I_o	Short circuit output current		50	mA
P_{tot}	Total power dissipation		1	W

* Stresses grater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification in not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONNECTIONS



BLOCK DIAGRAM



RECOMMENDED DC OPERATING CONDITIONS

($T_A = 0$ to 70°C)

	PARAMETER	VALUES			UNIT	NOTES
		min	typ	max		
V_{DD}	Supply voltage	10.8	12	13.2	V	2
V_{CC}	Supply voltage	4.5	5	5.5	V	2,3
V_{SS}	Supply voltage	0	0	0	V	2
V_{BB}	Supply voltage	−4.5	−5	−5.7	V	2
V_{IHC}	Input high voltage on $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7	V	2
V_{IH}	Input high voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.2		7	V	2
V_{IL}	Input low voltage, all inputs	−1		0.8	V	2

DC ELECTRICAL CHARACTERISTICS

($T_A = 0$ to 70°C) ($V_{DD} = 12V \pm 10\%$) ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $V_{BB} = -5.7$ to $-4.5V$)

	PARAMETER	VALUES			UNIT	NOTES
		min.	typ.	max.		
I_{DD1}	Average V_{DD} power supply current			35	mA	5
I_{DD2}	Standby V_{DD} power supply current			2	mA	8
I_{DD3}	Average V_{DD} power supply current during „$\overline{RAS}$ only" cycles			25	mA	
I_{CC}	V_{CC} power supply current				mA	6
I_{BB}	Average V_{BB} power supply current			150	µA	
$I_{I(L)}$	Input leakage current (any input)			10	µA	7
$I_{O(L)}$	Output leakage current			10	µA	8,9
V_{OH}	Output high voltage ($I_{SOURCE} = -5mA$)	2.4			V	
V_{OL}	Output low voltage ($I_{SINK} = 3.2$ mA			0.4	V	

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(T_A = 0 to 70°C) (V_{DD} = 12V ± 10%) (V_{CC} = 5V ± 10%, V_{SS} = 0V, V_{BB} = -5.7 to -4.5V)

	PARAMETER	MMN 4027-2		MMN 4027-3		MMN 4027-4		UNIT	NOTE
		min.	max.	min.	max.	min.	max.		
t_{RC}	Random read or write cycle time	320		375		380		ns	
t_{RWC}	Read write cycle time	320		375		395		ns	
t_{RMW}	Read modify write cycle time	320		405		470		ns	
t_{RAC}	Access time from row adress strobe		150		200		250	ns	11-13
t_{CAC}	Access time from column address strobe		100		135		165	ns	12-13
t_{OFF}	Output buffer turn-off delay		40		50		60	ns	
t_{RP}	Row address strobe precharge time	100		120		120		ns	
t_{RAS}	Row address strobe pulse width	150	10000	200	10000	250	10000	ns	
t_{RSH}	Row address strobe hold time	100		135		165		ns	
t_{CAS}	Column address strobe pulse width	100		135		165		ns	
t_{CSH}	Column addreess strobe hold time	150		200		250		ns	
t_{RCD}	Row to column strobe delay	20	50	25	65	35	85	ns	14
t_{ASR}	Row address set-up time	0		0		0		ns	
t_{RAH}	Row address hold time	20		25		35		ns	
t_{ASC}	Column address set-up time	-10		-10		-10		ns	
t_{CAH}	Column address hold time	45		55		75		ns	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{CSC}	Chip select set-up time	-10		-10		-10		ns	
t_{CH}	Chip select hold time	45		55		75		ns	
t_{CHR}	Chip select hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_T	Transition time (rise and fall)	3	35	5	50	5	50	ns	15
t_{RCS}	Read command set-up time	0		0		0		ns	
t_{RCH}	Read command hold time	0		0		0		ns	
t_{WCH}	Write command hold time	45		55		75		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{WP}	Write command pulse width	45		55		75		ns	
t_{RWL}	Write command to row strobe lead time	50		70		85		ns	
t_{CWL}	Write command to column strobe lead time	50		70		85		ns	
t_{DS}	Data in set-up time	0		0		0		ns	16
t_{DH}	Data in hold-time	45		55		75		ns	16
t_{DHR}	Data in hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{CRP}	Column to row strobe precharge time	0		0		0		ns	
t_{CP}	Column precharge time	60		80		110		ns	
t_{RFSH}	Refresh period		2		2		2	ns	
t_{WCS}	$\overline{\text{Write command}}$ set-up time	0		0		0		ns	17
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	60		80		90		ns	17
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	110		145		175		ns	17
t_{DOH}	Data out hold time	10		10		10		ns	

CAPACITANCES

(T_A = 0 to 70°C , V_{DD} = 12V ± 10%, V_{SS} = 0V, V_{BB} = -5.7 to -4.5V)

	PARAMETER	VALUES typ.	VALUES max.	UNIT	NOTES
C_{I1}	Input capacitance (A_0-A_5, D_{IN}, $\overline{CS}$)	4	5	pF	18
C_{I2}	Input capacitance RAS, CAS, WRITE	8	10	pF	18
C_O	Output capacitance (D_{OUT})	5	7	pF	8-18

NOTES

1. Several cycles are requiered after power-up before proper device operation is achieved. Any 8 cycles wich perform refresh are adequate for this purpose.
2. All voltages referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.
3. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. T_{amb} is specified for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all AC parameters are met.
5. Current is proportional to cycle rate. I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min).
6. I_{CC} depends on output loading. The V_{CC} supply is connected to the output buffer only.
7. All device pins at 0 volts except V_{BB} wich is at -5V and the pin under test wich is at +10V.
8. Output is disabled (high-impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is requiered prior to measurement of this parameter.
9. $0V \leq V_{out} \leq +10V$.
10. AC measurement assume $t_T = 5ns$.
11. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
12. Assumes that $t_{RCD} \geq t_{RCD}$ (max)
13. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
14. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a referance point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
15. V_{IHC} (min)or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
16. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modifywrite cycles.
17. t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating parameters in a read/write or read/modify/write cycle only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min. the cycle is a read-write cycle and Data Out will contain data read from the selected, cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.
18. Effective capacitance is calculated from the equation :
$$C = \frac{\Delta Q}{\Delta V} \text{ with } \Delta V = 3 \text{ volts.}$$

ADDRESSING

The 12 address bits required to decode one of 4096 cell locations within the M 4027 are multiplexed onto the 6 address inputs and latched into the on-chip row and column address latches.
Row Address Strobe ($\overline{RAS}$) latches the six row address bits conto the chip. Column Address Strobe ($\overline{CAS}$) latches the six column address bits plus Chip Select ($\overline{CS}$) onto the chip.
Since the internal circuitry allows the columns information to be externally applied to the chip before it is actually required, the hold time requirements for column address and $\overline{CS}$ are also referenced to $\overline{RAS}$. However, this gates $\overline{CAS}$ feature allows the systems designer to compensate for timing skews that may be encountered in the multiplexing operation.
Since the Chip Select signal is not required until $\overline{CAS}$ time, which is well into the memory cycle, its decoding time does not add to system access or cycle time.
Additional timing margin is gained because column address is not required until $\overline{CAS}$ makes its negative transition.
The timing is further simplified by the positive transition of $\overline{CAS}$ not being referenced to the positive transition of $\overline{RAS}$. In fact, $\overline{CAS}$ need not go HIGH until the beginning of the next cycle.

DATA INPUT/OUTPUT

Data to be written into selected storage cell of the memory chip is first stored in the on-chip data latch. The gating of this latch is performed with a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active.
The later of this signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In into the latch. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is activated prior to $\overline{CAS}$, the Data In is strobe by $\overline{CAS}$, and set-up time and hold time are referenced to $\overline{CAS}$. If the Data In input is not available at $\overline{CAS}$ time or the cycle is a read-write or readmodify-write, the $\overline{WRITE}$ signal must be delayed until after $\overline{CAS}$. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$. (To illustrate this feature, Data In is re-

ferenced to $\overline{WRITE}$ in the timing diagram depicting the read-write and page mode write cycles while the "early write" cycle diagram shows Data in referenced to $\overline{CAS}$) Note that if the chip is unselected ($\overline{CS}$ high at $\overline{CAS}$ time) $\overline{WRITE}$ comands are not executed and, consequently, data stored in the memory is unaffected. Data is retrieved from the memory in read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of memory cycle in which $\overline{CAS}$ is active. Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

At the beginning of a memory cycle, the state of the Data Out latch and buffer depend on the previous memory cycle.
Changes in the condition of Data Out latch are initiated by $\overline{CAS}$. The negative transition of $\overline{CAS}$ causes the Data Output (D_{OUT}) to unconditionnaly go to its open-circuit state. If will remain open-circuited until after the access D_{OUT} time, the will assume the proper state for the type of cycle performed.
If the cycle is read, read-modify-write, or a delayed write and the chip is selected, then the D_{OUT} latch and buffer will contain the data from the selected cell. This output data is the same polarity (not inverted)as the input data. If the cycle is a write cycle ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low) and the chip is selected, then D_{OUT} will contain the input data.
Once the D_{OUT} goes active, it will remain active until the next negative transition of $\overline{CAS}$.
If the cycle is a $\overline{CAS}$ only cycle (no $\overline{RAS}$ signal), then D_{OUT} will assume the open circuit state.
The same istrue for normal cycles (both $\overline{RAS}$ and $\overline{CAS}$ present-when the chip is unselected D_{OUT} remains in the open-circuit state until the next negative transition of $\overline{CAS}$.
$\overline{RAS}$ only refresh cycles (no $\overline{CAS}$) have no effect on the D_{OUT}.
However, when $\overline{Ras}$ only refresh cycles are continued for extended periods of time, D_{OUT} may eventually go open-circuit.
If the chip unselected, it will not accept a write command and the D_{OUT} will remain in the open-circuit state.

INPUT/OUTPUT LEVELS

All inputs, including the two address strobes, interface directly with TTL.
The high-impedance, low-capacitance input characteristics simplify input driver selection by allowing use of standard logic elements rather than specially designed driver elements
The 3-state output buffer is a low impedance to V_{CC} for a logic "1" and a low impedance to V_{SS} for a logic "0".
The output resistance to V_{CC} (logic "1" state) is 420 ohm maximum and 135 ohm tipically.
The output resistance to V_{SS} (logic "0" state) is 125 ohm maximum and 35 ohm tipically.
The separate V_{CC} pin allows the output buffer to be powered from supply voltage of the logic to wich chip is interfaced.
During battery stand-by operation, the V_{CC} pin may be unpowered without effecting the MMN 4027 refresh operation.

This allows all system logic, except $\overline{RAS}$ timing circuitry and refresh address logic, to be turned off during battery stand-by to save power.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row address every two millisecond or less.

Any cycle in which a $\overline{RAS}$ signal occurs, accomplished a refresh operation. A read cycle will refresh the selected row, regardless of the state of the Chip Select ($\overline{CS}$) input.
A write or read-modify-write cycle also refreshes the selected row, but the chip should be unseleced to prevent writing data into the selected cell.

If, during a refresh cycle, the MMN 4027 receives a $\overline{RAS}$ signal but no $\overline{CAS}$ signal, the state of the output will not be affected. However, if "$\overline{RAS}$-only" refresh cycles (when $\overline{RAS}$ is the only signal applied to the chip) are contained for extended periods, the output buffer may eventually lose proper data and go open-circuit.

The output buffer will regain activity with the first cycle in which a $\overline{CAS}$ signal is applied to the chip.

POWER DISSIPATION/STANDBY MODE

Most of the circuitry used in the MMN 4027 and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle.
Tipically, the power is 170 mW at 1 μsec cycle rate for MMN 4027 with a worse case power of less than 470 mW at 320 μsec cycle time.

To reduce the overall system power, the Row Address Strobe ($\overline{RAS}$) should be decoded and supplied to only the selected chips.

The $\overline{CAS}$ must be supplied to all chips (to turn of the unselected output.).

Those chips that did not receive a $\overline{RAS}$, however will not dissipate any power on the $\overline{CAS}$ edges, except for that requiered to turn off the outputs.

If the $\overline{RAS}$ signal is decoded and supplied only the selected chips, then the chip select ($\overline{CS}$) input of all chips can be at a logic 0.

Then chips that receive a $\overline{CAS}$ but no, $\overline{RAS}$ will be unselected (output open-circuited) regardless of the Chip Select input.

For refresh cycles, however, either the $\overline{CS}$ input for all chips must be high or the $\overline{CAS}$ input must be held high to prevent several "wire-OR" outputs from turning on with opposing force. Note that the MMN 4027 will dissipate considerably less power when the refresh operation is accomplished with a "$\overline{RAS}$-only" cycle as opposed to a normal $\overline{RAS}/\overline{CAS}$ memory cycle.

PAGE MODE OPERATION

The "Page mode" feature of the MMN 4027 allows for succesive memory operations at multiple column location of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and keeping the $\overline{RAS}$ signal at logic 0 throughout all succesive memory cycles in which the row address is common.
This "Page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. The time requiered for strobing in a new row address is eliminated thereby decreasing the access and cycle times. The chip select input ($\overline{CS}$) is operative in page mode cycles just as in normal cycles. It is not ecessary that the chip be selected during the first operation in sequence of page cycles.

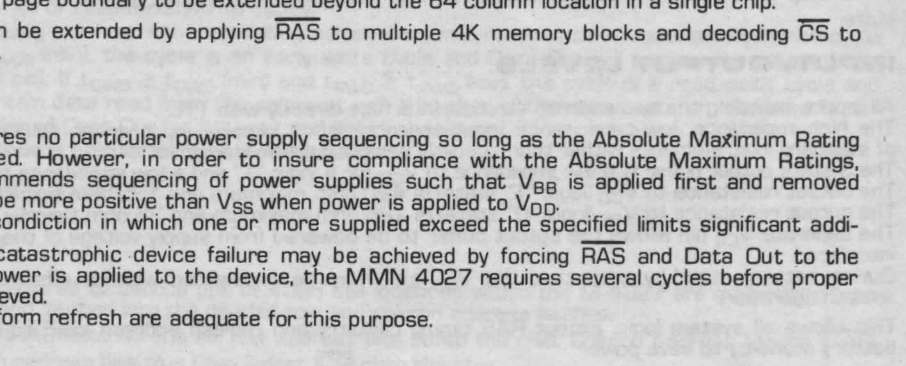
Likewise, the $\overline{CS}$ input can be used to select or disable any cycle (s) in a series of page cycles. This feature allows the page boundary to be extended beyond the 64 column location in a single chip.

The page boundary can be extended by applying $\overline{RAS}$ to multiple 4K memory blocks and decoding $\overline{CS}$ to select the proper block.

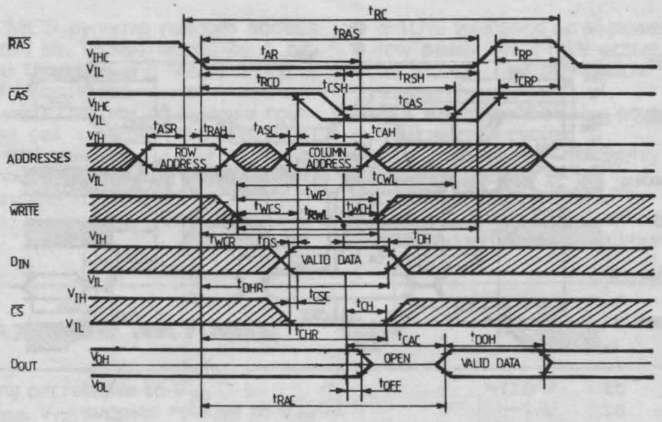
POWER UP

The MMN 4027 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, Microelectronica recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.
Under system failure condiction in which one or more supplied exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and Data Out to the inactive state. After power is applied to the device, the MMN 4027 requires several cycles before proper device operation is achieved.
Any 8 cycles which perform refresh are adequate for this purpose.

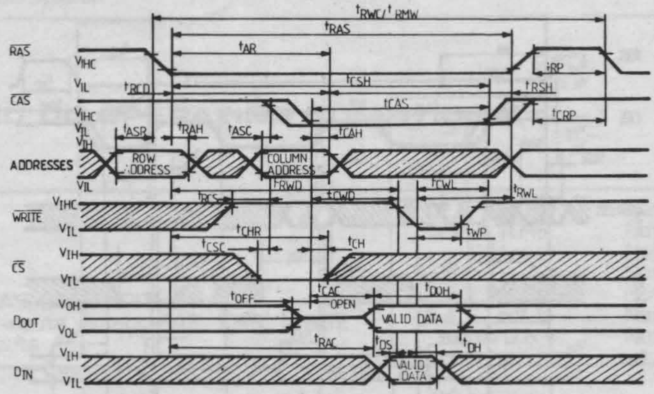
READ CYCLE



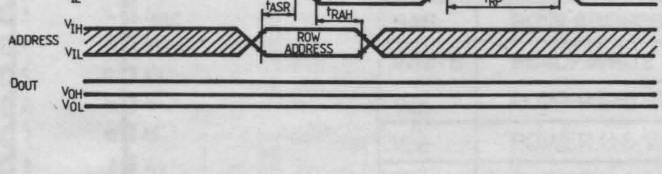
WRITE CYCLE
(early write)



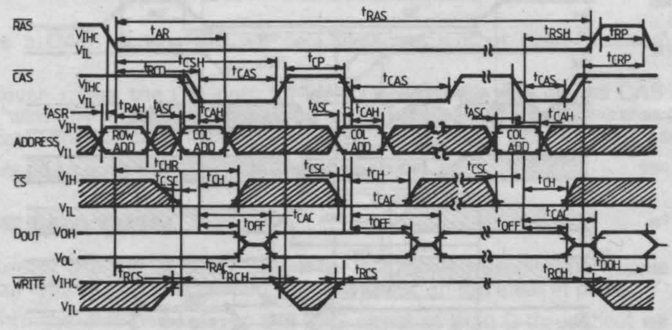
READ WRITE / READ MODIFY-WRITE CYCLE



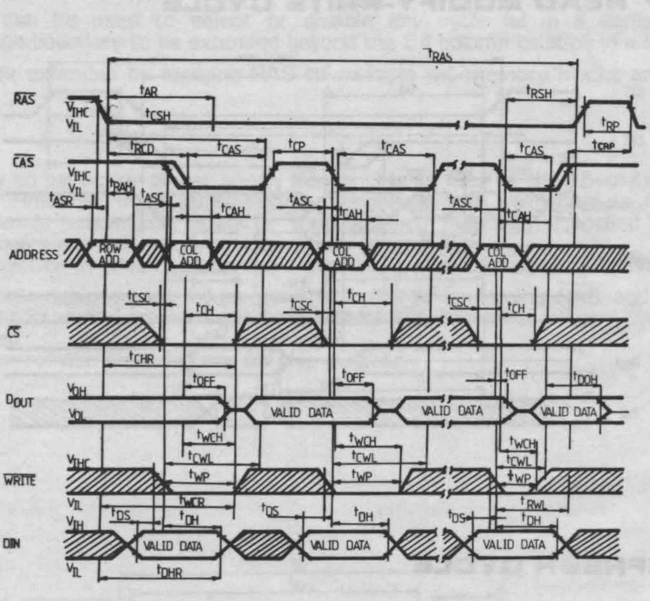
$\overline{RAS}$ ONLY REFRESH CYCLE



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



16384-BIT DYNAMIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION

The MMN 4116 is a MOS dynamic random access memory circuit organized as 16384 words by 1 bit. The technology used to fabricate the MMN 4116 is double-poly N-channel silicon gate.

This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability.

Multiplexed address inputs permit the MMN 4116 to be packaged in a standard 16-pin DIP.

FEATURES

- ±10% tolerance on all power supplies (+12 V, ±5 V)
- low power: 462 mW active, 20 mW standby (max)
- all inputs TTL compatible and protected against static charge.
- ECL compatible on V_{BB} power supply (−5·7 V)
- 128 refresh cycles
- read-modify-write, RAS-only refresh, and page-mode capability
- output data controlled by CAS and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary

ABSOLUTE MAXIMUM RATINGS

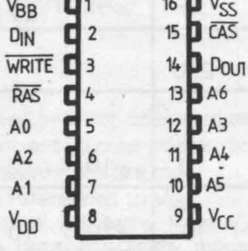
	Voltage on any pin relative to V_{BB}	−0.5 V	to	+20 V
	Voltage on V_{DD}, V_{CC} supplies relative to V_{SS}	−1 V	to	+15 V
	$V_{BB}-V_{SS}$ ($V_{DD}-V_{SS}>0$)			0V
T_A	Operating temperature	0°C	to	+70°C
T_{stg}	Storage temperature	−55°C	to	+125°C
I_o	Short circuit output current			50 mA
P_{tot}	Total power dissipation			1 W

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0 to 70°C)[1]

V_{DD} supply voltage	12 V ± 10%	Note 2
V_{CC} supply voltage	5 V ± 10%	Note 2,3
V_{SS} supply voltage	0 V	Note 2
V_{BB} supply voltage	−5.7 V to − 4.5 V	Note 2
Input high voltage on RAS, CAS, WRITE	2.7 V to 7 V	Note 2
Input high voltage, all inputs except RAS, CAS, WRITE	2.4 V to 7 V	Note 2
Input low voltage, all inputs	−1 V to 0.8 V	Note 2

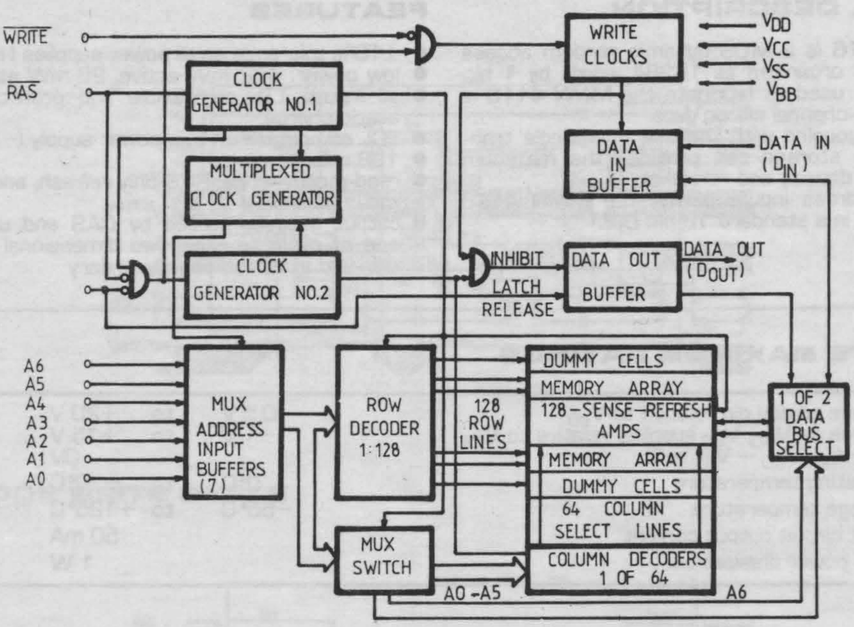
PIN CONNECTIONS



PIN NAMES

$A_0 - A_6$	ADDRESS INPUTS
CAS	COLUMN ADDRESS STROBE
DIN	DATA IN
D_{OUT}	DATA OUT
RAS	ROW ADDRESS STROBE
WRITE	READ/WRITE INPUT
V_{BB}	POWER (−5 V)
V_{CC}	POWER (+5 V)
V_{DD}	POWER (+12 V)
V_{SS}	GROUND

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

(T_A = 0 to 70°C)[1], (V_{DD} = 12V ± 10%; V_{BB} = -5.7 to -4.5V; V_{SS} = 0V; V_{CC} = 5V ± 10%)

PARAMETER		TEST CONDITIONS	MMN 4116-2/3 min	MMN 4116-2/3 max	MMN 4116-4 min	MMN 4116-4 max	UNIT	NOTE
I_{DD1}	Average operating current	$\overline{RAS}$, $\overline{CAS}$ cycling		35		35	mA	4
I_{CC1}	Average operating current							5
I_{BB1}	Average operating current	$t_{RC} = t_{RC}$ (min)		200		200	μA	
I_{DD2}	Standby current	$\overline{RAS} = V_{IHC}$		1.5		1.5	mA	
I_{CC2}	Standby current	D_{OUT} = High impedance	-10	10	-10	10	μA	
I_{BB2}	Standby current			100			μA	
I_{DD3}	Refresh average current	Refresh mode: $\overline{RAS}$ cycling		27		27	mA	4
I_{CC3}	Refresh average current	$\overline{CAS} = V_{IHC}$	-10	10	-10	10	μA	
I_{BB3}	Refresh average current	$t_{RC} = t_{RC}$ (min)		200			μA	
I_{DD4}	Page mode average current	Page mode: $\overline{RAS} = V_{IL}$		27		27	mA	4
I_{CC4}	Page mode average current	$\overline{CAS}$ cycling					A	5
I_{BB4}	Page mode average current	$t_{PC} = t_{PC}$ (min)		200			μA	
$I_{I(L)}$	Input leakage current	V_{BB} = −5 V 0V ≤ V_{IN} ≤ +7 V, all other pins not under test = 0V	−10	10	−10	10	μA	
$I_{O(L)}$	Output leakage current	D_{OUT} is disabled 0V ≤ V_{OUT} ≤ +5.5 V	−10	10	−10	10	μA	
V_{OH}	Output high voltage	I_{OUT} = −5 mA	2.4		2.4		V	3
V_{OL}	Output low voltage	I_{OUT} = 4.2 mA		0.4		0.4	V	3

AC ELECTRICAL CHARACTIRISTICS AND RECOMMENDED OPERATING CONDITIONS

($T_A = 0$ to $70°C$)[1], ($V_{DD} = 12\ V \pm 10\%$; $V_{CC} = 5\ V \pm 10\%$; $V_{SS} = 0\ V$; $V_{BB} = -5.7$ to $-4.5\ V$)

	PARAMETER	MMN 4116-2		MMN 4116-3		MMN 4116-4		UNIT	NOTES
		min	max	min	max	min	max		
t_{RC}	Random read or write cycle time	320		375		410		ns	9
t_{RWC}	Read-write cycle time	320		375		425		ns	9
t_{RMW}	Read modify write cycle time	320		405		500		ns	9
t_{PC}	Page mode cycle time	170		225		275		ns	9
t_{RAC}	Access time from $\overline{\text{RAS}}$		150		200		250	ns	10,12
t_{CAC}	Access time from $\overline{\text{CAS}}$		100		135		165	ns	11,12
t_{OFF}	Output buffer turn-off delay	0	40	0	50	0	60	ns	13
t_T	Transition time (rise and fall)	3	35	3	50	3	50	ns	8
t_{RP}	$\overline{\text{RAS}}$ precharge time	100		120		150		ns	
t_{RAS}	$\overline{\text{RAS}}$ pulse width	150	10000	200	10000	250	10000	ns	
t_{RSH}	$\overline{\text{RAS}}$ hold time	100		135		165		ns	
t_{CSH}	$\overline{\text{CAS}}$ hold time	150		200		250		ns	
t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	20	50	25	65	35	86	ns	14
t_{CRP}	CAS to $\overline{\text{RAS}}$ precharge time	−20		−20		−20		ns	
t_{ASR}	Row address set-up time	0		0		0		ns	
t_{RAH}	Row address hold time	20		25		35		ns	
t_{ASC}	Column address set-up time	−10		−10		−10		ns	
t_{CAH}	Column address hold time	45		55		75		ns	
t_{AR}	Column address hold time referenced to $\overline{\text{RAS}}$	95		120		160		ns	
t_{RCS}	Read command set-up time	0		0		0		ns	
t_{RCH}	Read command hold time	0		0		0		ns	
t_{WCH}	Write command hold time	45		55		75		ns	
t_{WCR}	Write command hold time referenced to $\overline{\text{RAS}}$	95		120		160		ns	
t_{WP}	Write command pulse width	45		55		75		ns	
t_{RWL}	Write command to $\overline{\text{RAS}}$ lead time	50		70		85		ns	
t_{CWL}	Write command to $\overline{\text{CAS}}$ lead time	50		70		85		ns	
t_{DS}	Data-in set-up time	0		0		0		ns	15
t_{DH}	Data-in hold time	45		55		75		ns	15
t_{DHR}	Data-in hold time referenced to $\overline{\text{RAS}}$	95		120		160		ns	
t_{CP}	CAS precharge time (for page mode cycle only)	60		80		100		ns	
t_{REF}	Refresh period		2		2		2	ms	
t_{WCS}	$\overline{\text{WRITE}}$ command set-up time	−20		−20		−20		ns	16
t_{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ delay	60		80		90		ns	16
t_{RWD}	RAS to $\overline{\text{WRITE}}$ delay	110		145		175		ns	16

NOTES

1. T_A is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention.However, the V_{OH} (min) specification is not guaranteed in this mode.
4. I_{DD1}, I_{DD3} and I_{DD4} depend on cycle rate.

5. I_{CC1} and I_{CC4} depend upon output loading. During read out of high level data V_{CC} is connected through a low impedance to data out. At all other times I_{CC} consists of leakage currents only.
6. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
7. AC measurements assume $t_T = 5$ ns.
8. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
9. The specifications for t_{RC} (min) and t_{RWC} (min) t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_{amb} \leq 70°C$) is assured.
10. Assuming that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
11. Assuming that $t_{RCD} \geq t_{RCD}$ (max).
12. Measured with a load equivalent to 2 TTL loads and 100 pF.
13. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
14. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is exclusively controlled by t_{CAC}.
15. These parameters are eferenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and data output pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta v = 3$ volts and power supplies at nominal levels.
18. $\overline{CAS} = V_{IHC}$ to disable D_{OUT}.

DESCRIPTION

System oriented features include ±10% tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MMN 4116 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the MMN 4116 is capable of delayed write cycles, page-mode operation and RAS-only refresh. Proper control of the clock inputs (RAS, CAS and WRITE) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

ADDRESSING

The 14 address bits required to decode 1 of the 16,384 cell locations within the MMN 4116 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 7 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 7 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information. Note that CAS can be activated at any time after t_{RAH} and it will have no effect on the worst case data acces time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end-points result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max.) No data storage or reading errors will result if $\overline{CAS}$ is applied to the MMN 4116 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and access time from $\overline{RAS}$ will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of WRITE and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to CAS. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$). Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MMN 4116 is the high impedance (open-circuit) state. That is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition. If the memory cycle in progress is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active, the output will remain valid until $\overline{CAS}$ is taken to the precharge (logic 1) state, whether or not $\overline{RAS}$ goes into precharge.

If the cycle in progress is an "early-write" cycle ($\overline{WRITE}$ active before $\overline{CAS}$ goes active), then the output pin will maintain the high impedance state throughout the entire cycle. Note that with this type of output configuration, the user is given full control of the D_{OUT} pin simply by controlling the placement of $\overline{WRITE}$ command during a write cycle, and the pulse width of the Column Address. Strobe during read operations. Note also that even through data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle).

This type of output operation results in some very significant system implications.

Common I/O Operation — If all write operations are handled in the "early write" mode, then D_{IN} can be connected directly to D_{OUT} for a common I/O data bus.

D_{OUT} will remain valid during a read cycle from t_{CAC} until $\overline{CAS}$ goes back to a high level (precharge), allowing data to be valid from one cycle up until a new memory cycle begins with no penalty in cycle time. This also makes the $\overline{RAS}/\overline{CAS}$ clock timing relationship very flexible.

Two Methods of Chip Selection — Since D_{OUT} is not latched, $\overline{CAS}$ is not required to turn off the outputs of unselected memory devices in a matrix. This means that both $\overline{CAS}$ and/or $\overline{RAS}$ can be decoded for chip selection. If both $\overline{RAS}$ and $\overline{CAS}$ are decoded, then a two dimensional (X, Y) chip select array can be realized.

Extended Page Boundary — Page — mode operation allows for successive memory cycles at multiple column locations of the same row address. By decoding $\overline{CAS}$ as a page cycle select signal, the page boundary can be extended beyond the 128 column location in a single chip. (See page-mode operation).

OUTPUT INTERFACE CHARACTERISTICS

The three state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 420 Ω maximum and 135 Ω typically. The resistance to V_{SS} (logic 0 state) is 95 Ω maximum and 35 Ω typically.

The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MMN 4116 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

PAGE MODE OPERATION

The "Page Mode" feature of the MMN 4116 allows for successive memory operations at multiplie column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page-mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

The page boundary of a single MMN 4116 is limited to the 128 column locations determined by all combinations of the 7 column address bits. However, in system applications which utilize more than 16,384 data words, (more than one 16K memory block), the page boundary can be extended by using $\overline{CAS}$ rather than $\overline{RAS}$ as the chip select signal. $\overline{RAS}$ is applied to all devices to latch the row address into each device and the $\overline{CAS}$ is decoded and serves as a page cycle select signal. Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ signals will execute a read or write cycle.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles. $\overline{RAS}$-only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{DD3} specification.

POWER CONSIDERATIONS

Most of the circuitry used in the MMN 4116 is dynamic and most of the power drawn is the result of an address strobe edge.
Consequently, the dynamic power is primarily a function of operating frequency rather than active duty cycle. This current characteristic of the MMN 4116 precludes inadvertent burn out of the device in the event that the clock inputs become shorted to ground due to system malfunction.
Although no particular power supply noise restriction exists other than the supply voltages remain within the specified tolerance limits, adequate decoupling should be provided to suppress high frequency noise resulting from the transient current of the device. This insures optimum system performance and reliability, Bulk capacitance requirements are minimal since the MMN 4116 draws very little steady state (DC) current.
In system applications requiring lower power dissipations, the operating frequency (cycle rate) of the MMN 4116 can be reduced and the (guaranteed maximum) average power dissipation of the device will be lowered in accordance with the I_{DD1} (max) spec limit equation.

Note: The MMN 4116 is guaranteed to have a maximum I_{DD1} requirement with an ambient temperature from 0° to 70°C.
1 microsecund cycle, results in a reduced maximum I_{DD1} requirement of under 20 mA with an ambient temperature range from 0° to 70°C.
Although $\overline{RAS}$ and/or $\overline{CAS}$ can be decoder and used as a chip select signal for the MMN 4116 overall system power is minimized if the Row Address Strobe ($\overline{RAS}$) is used for this purpose. All unselected devices (those which do not receive a $\overline{RAS}$) is used for this purpose. All unselected devices (those which do not receive a $\overline{RAS}$) will remain in a low power (standby) mode regardless of the state of $\overline{CAS}$.

POWER UP

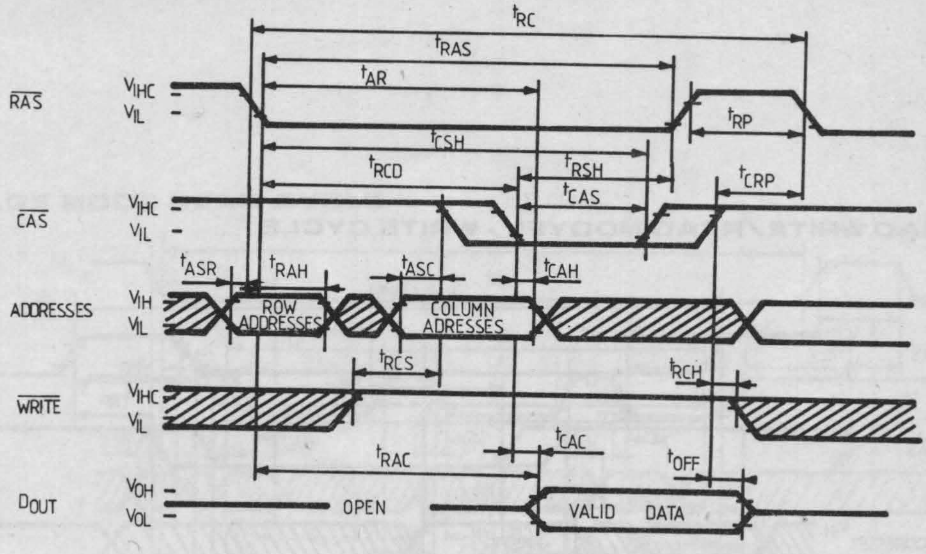
The MMN 4116 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, MICROELECTRONICA recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.
Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and $\overline{CAS}$ to the inactive state (high level).
After power is applied to the device, the MMN 4116 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

CAPACITANCES

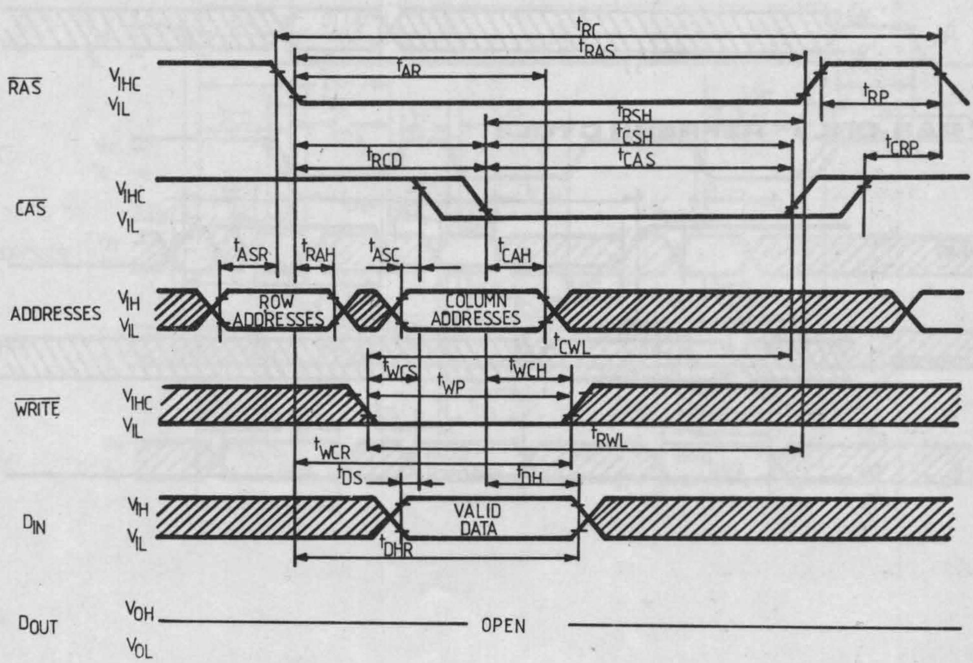
(T_{amb} = 0 to 70°C; V_{DD} = 12 V ± 10%; V_{BB} = -5.7 to -4.5 V; V_{SS} = 0V)

	PARAMETER	RATING min	RATING typ	RATING max	UNIT	NOTES
C_{i1}	Input capacitance (A_0—A_6) DIN		4	5	pF	17
C_{i2}	Input capacitance RAS, CAS, WRITE		8	10	pF	17
C_o	Output capacitance (D_{OUT})		5	7	pF	17,18

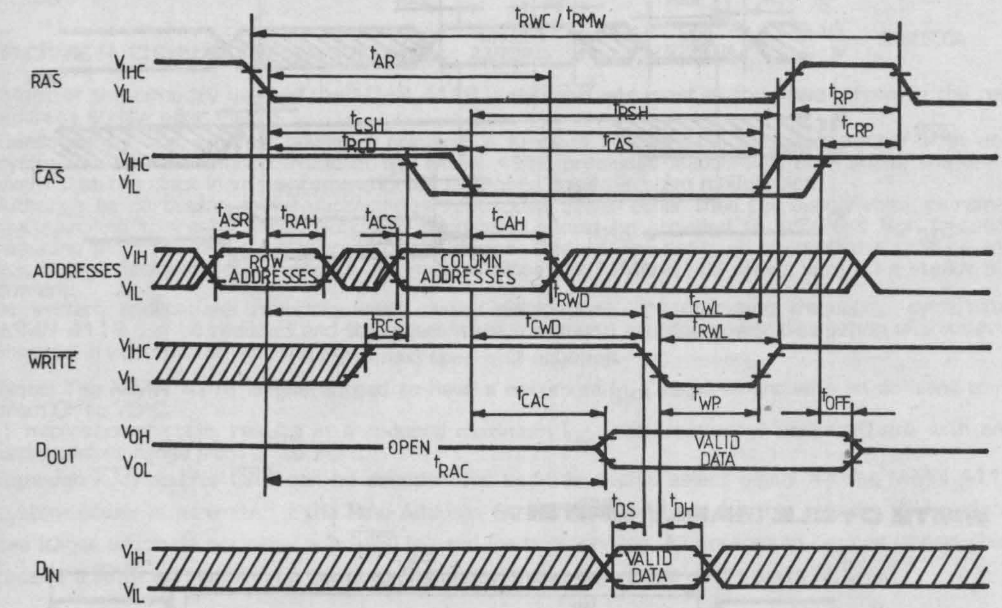
READ CYCLE



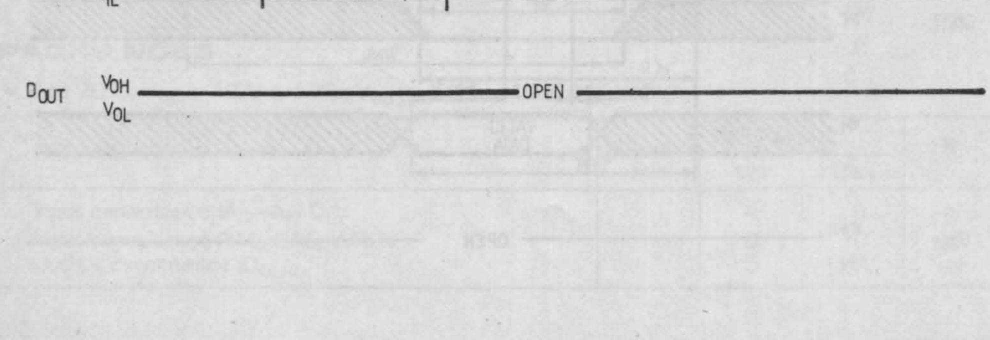
WRITE CYCLE (EARLY WRITE)



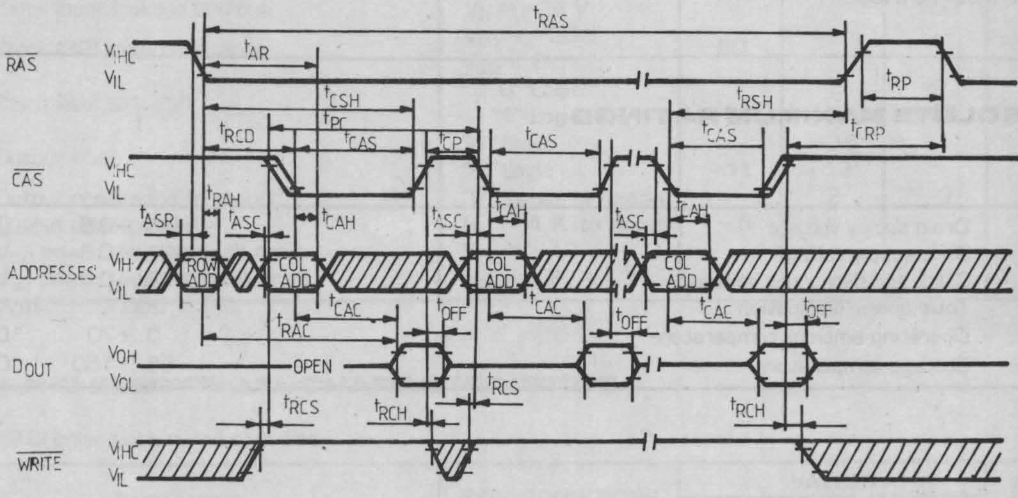
READ WRITE/READ MODYFY - WRITE CYCLE



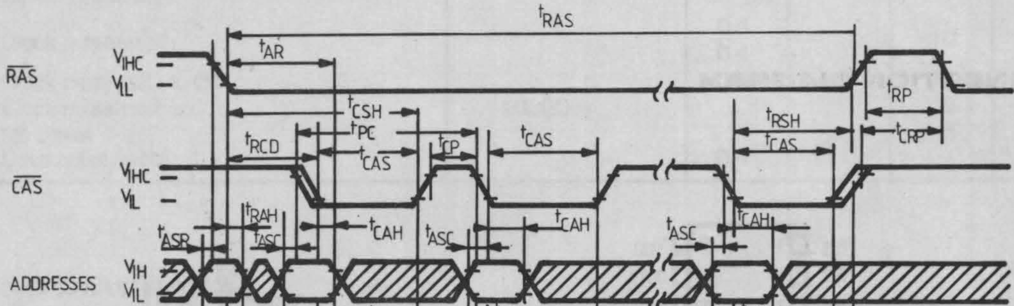
"$\overline{\text{RAS}}$-ONLY" REFRESH CYCLE



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



DUAL 16 BIT STATIC SHIFT REGISTER

GENERAL DESCRIPTION

MMP 02 is a dual 16 bit static shift register. It is a monolithic integrated circuit manufactured in standard Al-gate PMOS technology.
The circuit is designed to operate on a two phase clock, Ø1 and Ø2.
For DC storage conditions, Ø1 must be a logic "0" and Ø2 must be a logic "1"

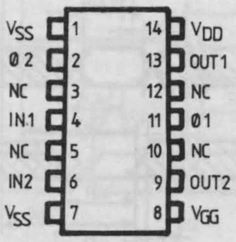
FEATURES

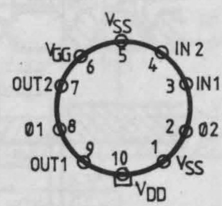
- Two phase clock
- High speed operation DC to 1 MHz
- Low power consummption

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Drain supply voltage	−30...+0.3	V
V_{GG}	Gate supply voltage	−30...+0.3	V
$V_Ø$, V_I	Clock and data input voltages	−30...+0.3	V
P_{tot}	Total power dissipation	200	mW
T_A	Operating ambient temperature	0...+70	°C
T_{stg}	Storage temperature	−55...+150	°C

CONNECTION DIAGRAM





STATIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$ unless otherwise specified)

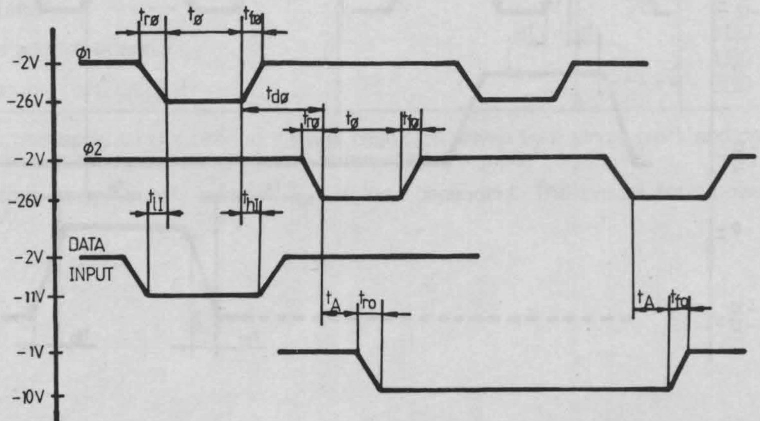
PARAMETER		TEST CONDITIONS	VALUES			UNIT
			min.	typ.	max.	
V_{IL}	Data input level	"0" Logic			−2	V
V_{IH}	Data input level	"1" Logic	−10			V
I_{LI}	Data input leakage current	$V_I = -20$ V			1	μA
$I_{LØ}$	Clock input leakage current	$V_Ø = -26$ V			100	μA
$R_{IØ2}$	Clock (Ø2) input resistance	$V_{Ø1} = -26$ V, $V_{Ø2} = 0$	60			KΩ
$V_{ØL}$	Clock level (Ø1, Ø2)	"0" Logic			−2	v
$V_{ØH}$		"1" Logic	−26		−28	V
V_{OL}	Output level	"0" Logic		−0.5	−1	V
V_{OH}		"1" Logic	−11	−12		V
R_{OL}	Output resistance to ground	"0" Logic at output		2	3	KΩ
V_{OC}	Output drive capability	R_L = 4 K to ground	−5			V
I_{DD}	V_{DD} power supplycurrent drain	$V_{DD} = -13$ V			12	mA
I_{GG}	V_{GG} power supply current drain	$V_{GG} = -27$ V			2	mA

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$) unless otherwise specified

PARAMETER		TEST CONDITIONS	VALUES			UNIT
			min.	typ.	max.	
$f_Ø$	Clock frequency		c.c. DC		1	MHz
$t_{Ø1}$	Clock pulse width		0.4		10	μs
$t_{Ø2}$			0.4			μs
$t_{dØ}$	Clock delay Ø2 vs. Ø1		0.01		10	μs
t_r	Clock pulse rise and	10...90%			5	μs
t_f	fall times				5	μs
t_D	Data pulse width		0.4			μs

TIMING DIAGRAM



64 BIT DYNAMIC SHIFT REGISTER

GENERAL DESCRIPTION

MMP 03 is a 64 bit dynamic shift register, manufactured in standard Al-gate PMOS technology.
The on-chip clock generator and a separate output buffer supply yield an output level inependent of clock frequency and amplitude.

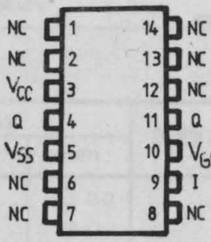
FEATURES

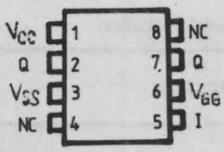
- Maximum operating frequency 1 MHz
- Operating with a single external phase
- TTL output compatible

ABSOLUTE MAXIMUM RATINGS

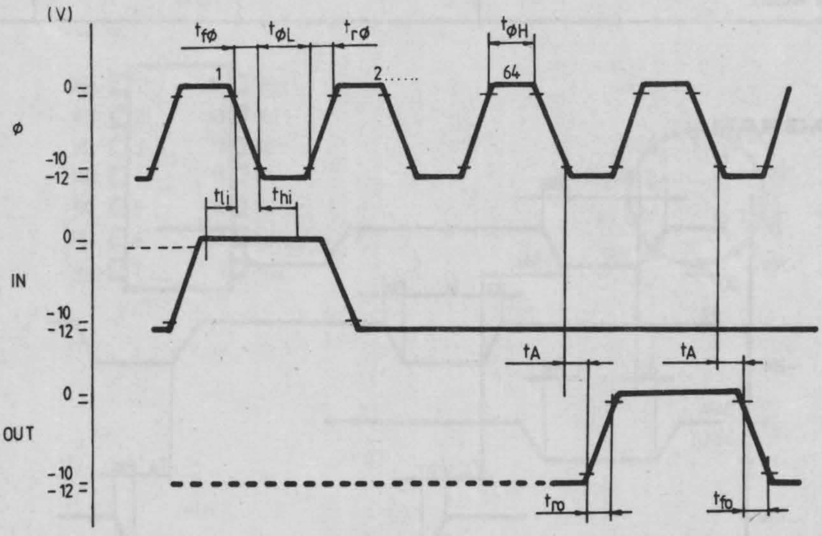
Voltage on any pin with respect to V_{SS}		−30...+0.3	V
P_{tot}	Total power dissipation	500	mW
T_A	Operating ambient temperature	0...+70	°C
T_{stg}	Storage temperature range	−55...+150	°C

PIN CONNECTIONS





TIMING DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(V_{GG} = −26...−28 V, V_{DD} = −12...−14 V, T_A = 0...+70°C, standard load 50 pF in parallel with 20 kohm, V_{SS} grounded)

	PARAMETER	TEST CONDITIONS	VALUES			UNIT
			min.	typ.	max.	
V_{GG}	Supply voltages		−28	−27	−26	V
V_{CC}			−28	−12	+0.3	V
V_{OL}	Output level		−0.5		0	V
V_{OH}			−14	−12	−10	V
$V_{\varnothing L}$	Clock signal level		−2		+0.3	V
$V_{\varnothing H}$			−28	−12	−9	V
V_{IL}	Data input level		−2		+0.3	V
V_{IH}			−28	−12	−9	V
$C_{\varnothing}$	Clock input capacitance	$V_{\varnothing}$ = 0		6	10	pF
I_{LI}	Data input leakage current	T_A = 25°C V_I = −15 V The other therminals at ground			1	μA
$I_{L\varnothing}$	Clock input leakage current	T_A = 25°C $V_{\varnothing}$ = −28 V The other terminals at ground			100	μA
R_{OH}	Output resistance (both	V_{DD} = −5 V		250	500	Ω
R_{OL}	output states)			250	500	Ω
I_{GG}	Power supply current (see note 2)	V_{GG} = −27 V $f_{\varnothing}$ = 1 MHz T_A = 25°C		5	6	mA

DYNAMIC ELECTRICAL CHARACTERISTICS

(V_{GG} = −26...−28 V, V_{CC} = −12...−14 V, T_A = 0...+70°C, standard load 50 pF in parallel with 20 kohm, V_{SS} grounded)

	PARAMETER	TEST CONDITIONS	VALUES			UNIT
			min.	typ.	max.	
$f_{\varnothing}$	Clock frequency		0.01		1	MHz
t_r	Clock rise and fall times	Note 1			100	ns
t_f					100	ns
t_{DS}	Data set-up time		20			ns
t_{DH}	Data hold time		75			ns
t_{rO}	Output rise and fall times			100		ns
t_{fO}				100		ns
t_A	Acces time			300		ns

Note 1: These limits apply to the case of several registers driven by a single clock and have to be observed for proper time positioning of the various output signals.

Note 2: The output power supply current, I_{CC}, is load dependent. The typical total power dissipation is 300 mW.

DUAL 3 - INPUT NOR GATE

GENERAL DESCRIPTION

The MMP 102 is a monolithic integrated circuit, available in 10 — lead dual in line plastic package. The MMP 102 is manufactured in P-channel MOS technology.

FEATURES

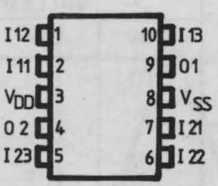
- High input resistance
- Inputs fully protected
- One supply voltage

ABSOLUTE MAXIMUM RATINGS

(All voltages relative to V_{SS})

V_{DD}	Drain supply voltage	−31...+0.3	V
V_I	Input voltage	−25...+0.3	V
T_A	Operating ambient temperature	0...+70	°C
T_{stg}	Storage temperature	−55...+125	°C

PIN CONNECTIONS



TRUTH TABLE

I_1	I_2	I_3	O
H	H	H	L
H	H	L	H
H	L	H	H
H	L	L	H
L	H	H	H
L	H	L	H
L	L	H	H
L	L	L	H

STATIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C) unless otherwise specified

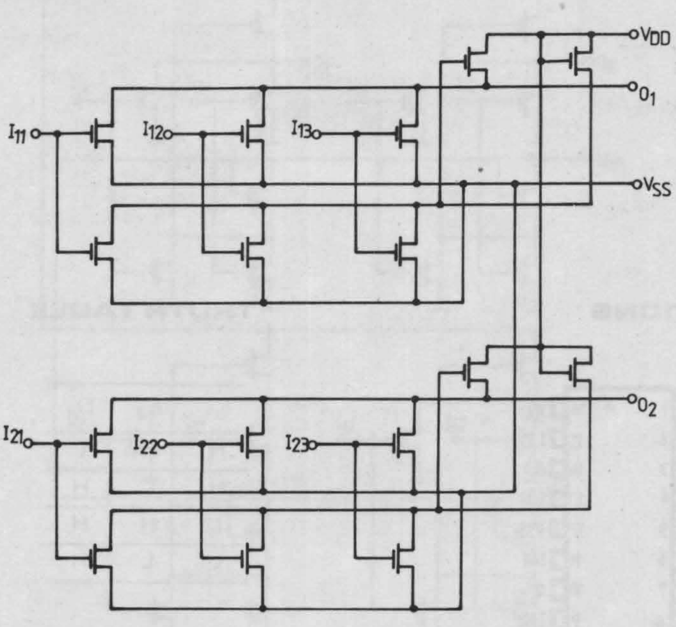
PARAMETER		TEST CONDITIONS	VALUES			UNIT
			min.	typ.	max.	
I_I	Input current	$+V_I = 25$ V	−10			μA
V_{OL}	Low level output voltage	$V_{IH} \geq -2$ V; $V_{IL} \leq -9$ V; $R_L = 1$ M			−10	V
V_{OH}	High level output voltage	$V_{IH} \geq -2$ V; $V_{IL} \leq -9$ V; $R_L = 100$ k	−1			V
V_{OL}	Low level output voltage at $I_O = +1$ mA	$V_{IH} \geq -2$ V; $V_{IL} \leq -9$ V			−5	V
V_{OH}	High level output voltage at $I_O = -1$ mA	$V_{IH} \geq -2$ V; $V_{IL} \leq -9$ V	−4			V
I_{DD}	Medium supply current	$R_L = 1$ M; $C_L = 60$ pF; $V_I = -12$ V; T/t = 2 : 1; f = 250 kHZ		−1		mA
C_I	Input capacitance	$V_{DD} = 0$ V; $V_I = 0.2$ V; f = 0.5...2 MHz			6	pF

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C) unless otherwise specified

PARAMETER		TEST CONDITIONS	VALUES			UNIT
			min.	typ.	max.	
t_{PHL}	Propagation delay time			300		ns
t_{PHL}	Propagation delay time			200		ns
C_{st}	Stray capacitance				30	pF

SCHEMATIC DIAGRAM



QUAD 2 - INPUT NOR GATE

GENERAL DESCRIPTION

The MMP 106 is a monolithic integrated circuit, available in 16 — lead dual in line plastic package. The MMP 106 is manufactured in P-channel MOS technology.

FEATURES

- High input resistance
- Inputs fully protected
- Two supply voltage

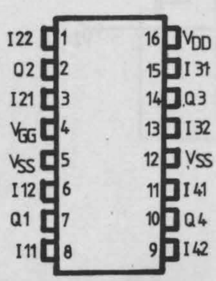
ABSOLUTE MAXIMUM RATINGS

V_{GG}	Gate supply voltage	−30...+0.3	V
V_{DD}	Drain supply voltage	−30...+0.3	V
V_I	Input voltage	−25...+0.3	V
T_A	Operating ambient temperature	0...+70	°C
T_S	Storage temperature	−55...+150	°C

RECOMMENDED OPERATING CONDITIONS

V_{GG}	Gate supply voltage	-27^{-1}_{+2}	V
V_{DD}	Drain supply voltage	$-13^{-0.5}_{+1.5}$	V

PIN CONNECTIONS



TRUTH TABLE

I_{n1}	I_{n2}	O_n
H	H	L
H	L	H
L	H	H
L	L	H

n = 1, 2, 3, 4

STATIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$) unless otherwise specified

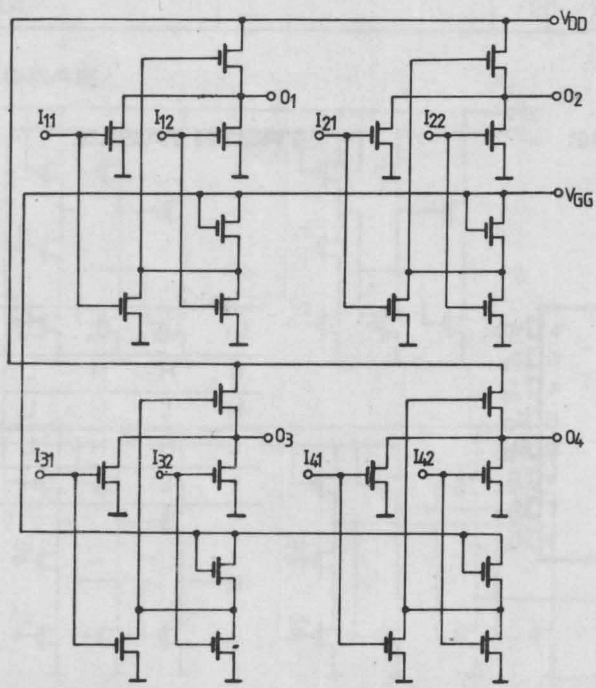
PARAMETER		TEST CONDITIONS	VALUES			UNIT
			min.	typ.	max.	
I_I	Input current	$V_I = -25$ V			10	µA
V_{OL}	Low level output voltage	$V_{IH} \geq -2$ V; $V_{IL} \leq -9$ V; $R_L = 1$ M	10			V
V_{OH}	High level output voltage	$V_{IH} \geq -2$ V; $V_{IL} \leq -9$ V; $R_L = 100$ K			1	V
V_{OL}	Low level output voltage at $I_O = +1$ mA	$V_{IH} \geq -2$ V; $V_{IL} \leq -9$ V	5			V
V_{OH}	High level output voltage at $I_O = -1$ mA	$V_{IH} \geq -2$ V; $V_{IL} \leq -9$ V			4	V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$) unless otherwise specified

PARAMETER		TEST CONDITIONS	VALUES			UNIT
			min.	typ.	max.	
t_{PLH}	Propagation delay time			320		ns
t_{PHL}	Propagation delay time			120		ns
C_{IN}	Input capacitance	$V_{GG} = V_{DD} = 0$ V; $V_I \geq 0.2$ V; f = 0.5...2 MHz			1	pF
C_{st}	Stray capacitance		30			pF

SCHEMATIC DIAGRAM



QUAD 2 - INPUT AND (NAND) GATE

GENERAL DESCRIPTION

The MMP 107 is a monolithic integrated circuit, available in 16 — lead dual in line plastic package.
The MMP 107 is manufactured in P-channel MOS technology.

FEATURES

- High input resistance
- Inputs fully protected
- Two supply voltages

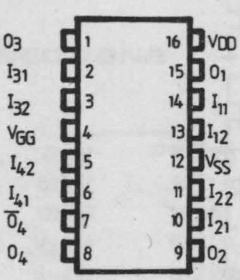
ABSOLUTE MAXIMUM RATINGS

V_{GG}	Gate supply voltage	−31...+0.3	V
V_{DD}	Drain supply voltage	−31...+0.3	V
V_I	Input voltage	−25...+0.3	V
T_A	Operating ambient temperature	0...+70	°C
T_{stg}	Storage temperature	−55...+150	°C

RECOMMENDED OPERATING CONDITIONS

V_{GG}	Gate supply voltage	-27^{-1}_{+2}	V
V_{DD}	Drain supply voltage	$-13^{-0.5}_{+1.5}$	V

PIN CONNECTIONS



TRUTH TABLE

I_{n1}	I_{n2}	O_n	$\overline{O}_4$
H	H	H	L
H	L	H	L
L	H	H	L
L	L	L	H

n = 1, 2, 3, 4

STATIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$) unless otherwise specified

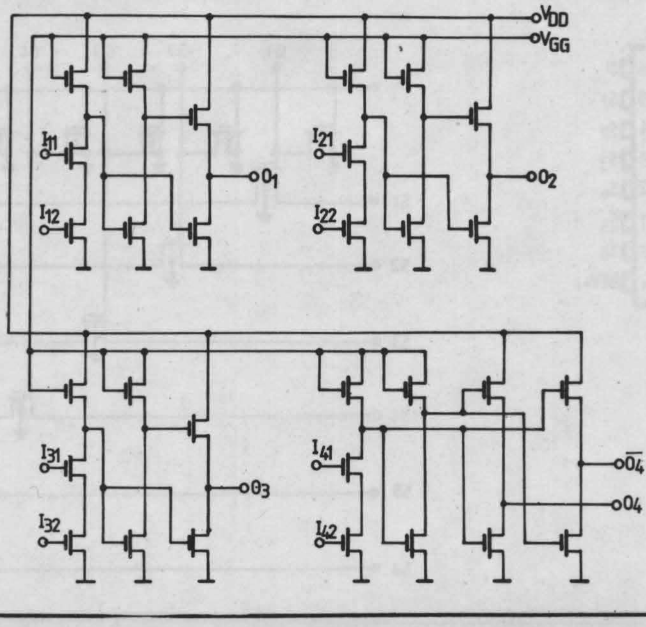
PARAMETER		TEST CONDITIONS	VALUES min.	VALUES typ.	VALUES max.	UNIT
I_I	Input current	$V_I = -25$ V			10	μA
V_{OL}	Low level output voltage	$V_{IH} \geq -2$ V; $V_{IL} \leq -9$ V; $R_L = 1$ MΩ	10			V
V_{OH}	High level output voltage	$V_{IH} \geq -2$ V; $V_{IL} \leq -9$ V; $R_L = 100$ KΩ			1	V
V_{OL}	Low level output voltage at $I_O = +1$ mA	$V_{IH} \geq -2$ V; $V_{IL} \leq -9$ V	5			V
V_{OH}	High level output voltage at $I_O = -1$ mA	$V_{IH} \geq -2$ V; $V_{IL} \leq -9$ V			4	V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$) unless otherwise specified

PARAMETER		TEST CONDITIONS	VALUES min.	VALUES typ.	VALUES max.	UNIT
t_{PLH}	Propagation delay time for 01...03, $\overline{04}$			320		ns
t_{PLH}	Propagation delay time for 04			150		ns
t_{PHL}	Propagation delay time			200		ns
C_{IN}	Input capacitance	$V_{GG} = V_{DD} = 0$ V; $V_I \geq 0.2$ V; $f = 0.5...2$ MHz			6	pF
C_{st}	Stray capacitance for 01...03, $\overline{04}$		30			pF
C_{st}	Stray capacitance 04		20			pF

SCHEMATIC DIAGRAM



6-CHANNEL ANALOG SWITCH

GENERAL DESCRIPTION

The MMP 115 contains six enhancement-mode P-channel MOS FETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 30 V peak-to-peak. The switches are integrated on a silicon substrate (body). The switches have a cannon drain terminal (D) which will function equally well as a common source. In the same manner, the source terminals. (S) will function equally well as drains. Each gate (G) is provided with a normally OFF "pull-up" MOS FET which may be turned ON to provide a current source to the gate-driving circuit. The pull-ups are turned ON or OFF by connecting the "P" terminal to a negative supply or to the "B" terminal respectively.

FEATURES

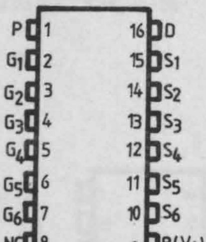
- Drain-source ON resistance 100 ohms
- Maximum switched voltage ±30V
- Maximum voltage in each terminal to, substrate −30 V
- All inputs protected

ABSOLUTE MAXIMUM RATINGS

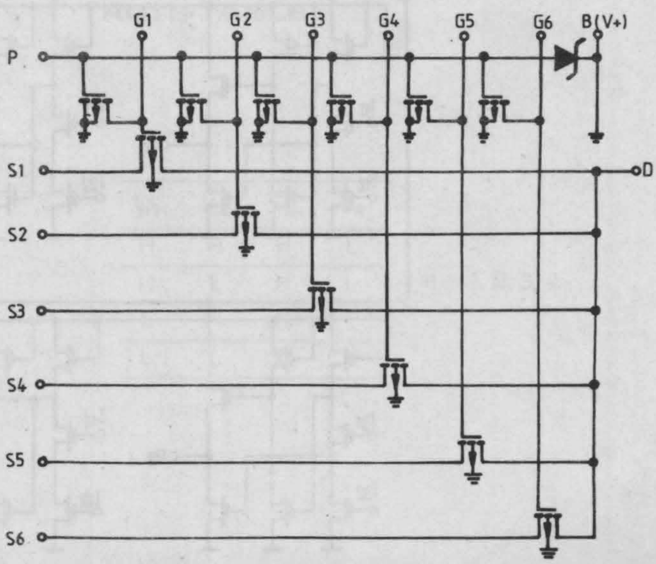
Bulk to source voltage	V_{BS}	−2 to +30	V
Bulk to drain voltage	V_{BD}	+30	V
Drain to source voltage	V_{DS}	±30	V
Bulk to gate voltage	V_{BG}	+35	V
Bulk to P terminal voltage	V_{BP}	+35	V
Drain, source current	I_D, I_S	100	mA
Power disipation	P_d	600	mW*
		900	mW
Storage temperature	T_{stg}	−55°C to 150 °C	
Operating temperature	T_A	0°C to 70 °C	

* for ceramic package

PIN CONNECTIONS



SCHEMATIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS $T_A = 25°C$.

PARAMETER		TEST CONDITIONS	VALUES			UNIT
			min.	typ.	max.	
V_T	Threshold voltage	$I_D = -10\ \mu A$, $V_{SB} = V_{DG} = 0\ V$	−1.5		−4	V
BV_{DS}	Drain-source breakdown voltage	$I_D = -50\ \mu A$, $V_{GS} = V_{SB} = 0\ V$	−30			V
BV_{SD}	Source-drain breakdown voltage	$I_S = -10\ \mu A$, $V_{GD} = 0\ V$	−30			V
BV_{GB}	Gate-bulk breakdown voltage	$I_G = -10\ \mu A$,	−30			V
BV_{PB}	P terminal-bulk breakdown voltage	$I_P = -10\ \mu A$, $V_{GB} = 0\ V$	−30			V
r_{ON}	Drain-source on resistance	$I_S = -1\ mA$, $V_{DB} = 0\ V$ $V_{GD} = -30\ V$			125	Ω
		$I_S = -1 mA$, $V_{DB} = -10\ V$, $V_{GD} = -20\ V$			200	Ω
		$I_S = -1 mA$, $V_{DB} = -20\ V$ $V_{GD} = -10\ V$			650	Ω
$I_{S(OFF)}$	Source off leakage current	$V_{SD} = -20\ V$, $V_{GD} = 0\ V$			−5	nA
$I_{D(OFF)}$	Drain off leakage current	$V_{DS} = -20\ V$, $V_{GS} = 0\ V = V_{SB}$			−25	nA
$I_{G(ON)}$	Gate on current	$V_{GB} = -30\ V$, $V_{PB} = -30\ V$	−0.8		−3.4	mA
I_{GSS}	Gate-channel leakage current	$V_{GB} = -20\ V$			−5	nA

* $V_{DB} = 0\ V$, $V_{PB} = 0\ V$, unless otherwise specified

5-CHANNEL ANALOG SWITCH

GENERAL DESCRIPTION

The MMP 116 contains five enhancement-mode P-channel MOS FETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up 30 V peak-to-peak.
The switches are integrated on a silicon substrate. The switches have a common drain terminal (D) which will function equally well as a common source. In the same manner, the source terminal (S) will function equally well as drain. Each gate (G) is provided with a normally OFF pull-up MOS FET which may be turn on to provide a current source to the gate driving circuit. The pull-ups are turned ON or OFF by connecting the P terminal to a negative supply or to the B terminal respectively.

FEATURES

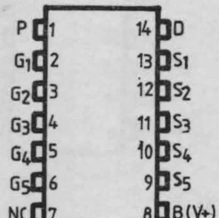
- Drain-source ON resistance 100 ohms
- Maximum switched voltage ±30V
- Maximum voltage in each terminal to, substrate −30 V
- All inputs protected

ABSOLUTE MAXIMUM RATINGS

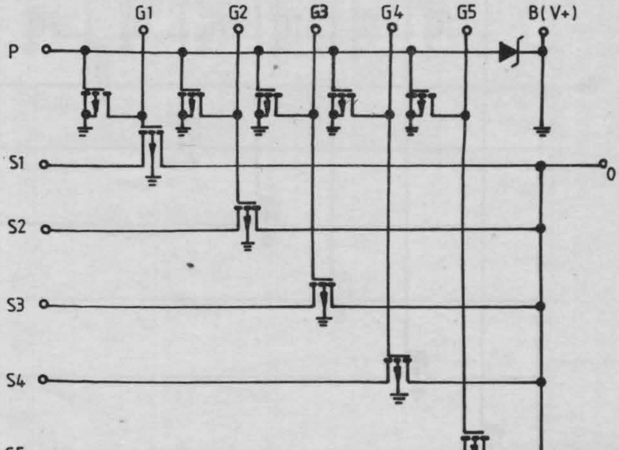
Bulk to source voltage	V_{BS}	+30 V
Bulk to drain voltage	V_{BD}	+30 V
Drain to source voltage	V_{DS}	±30 V
Bulk to gate voltage	V_{BG}	+35 V
Bulk to P terminal voltage	V_{BP}	+35 V
Drain, source current	I_D, I_S	100 mA
Power disipation	P_d	600 mW* 900 mW
Storage temperature	T_{stg}	−55°C to 150 °C
Operating temperature	T_A	0°C to 70 °C

* for ceramic package

PIN CONNECTIONS



SCHEMATIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS $T_A = 25°C$

PARAMETER		TEST CONDITIONS	VALUES min.	VALUES typ.	VALUES max.	UNIT
V_T	Threshold voltage	$I_D = -10\ \mu A$, $V_{SB} = V_{DG} = 0\ V$	−1.5		−4	V
BV_{DS}	Drain-source breakdown voltage	$I_D = -50\ \mu A$, $V_{GS} = V_{SB} = 0\ V$	−30			V
BV_{SD}	Source-drain breakdown voltage	$I_S = -10\ \mu A$, $V_{GD} = 0\ V$	−30			V
BV_{GB}	Gate-bulk breakdown voltage	$I_G = -10\ \mu A$,	−30			V
BV_{PB}	P terminal-bulk breakdown voltage	$I_P = -10\ \mu A$, $V_{GB} = 0\ V$	−30			V
r_{ON}	Drain-source on resistance	$I_S = -1\ mA$, $V_{DB} = 0\ V$ $V_{GD} = -30\ V$			125	Ω
		$I_S = -1mA$, $V_{DB} = -10\ V$, $V_{GD} = -20\ V$			200	Ω
		$I_S = -1mA$, $V_{DB} = -20\ V$ $V_{GD} = -10\ V$			650	Ω
$I_{S(OFF)}$	Source off leakage current	$V_{SD} = -20\ V$, $V_{GD} = 0\ V$			−5	nA
$I_{D(OFF)}$	Drain off leakage current	$V_{DS} = -20\ V$, $V_{GS} = 0\ V = V_{SB}$			−25	nA
$I_{G(ON)}$	Gate on current	$V_{GB} = -30\ V$, $V_{PB} = -30\ V$	−0.8		−3.4	mA
I_{GSS}	Gate-channel leakage current	$V_{GB} = -20\ V$			−5	nA

* $V_{DB} = 0\ V$, $V_{PB} = 0\ V$, unless otherwise specified

5-CHANNEL ANALOG SWITCHES

GENERAL DESCRIPTION

The MMP 117 contains six enhancement-mode P-channel MOS FETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 20 V peak-to-peak.
The switches are integrated on a silicon substrate (body). The drains of five of the switches are internally connected to the source of the sixth switch. This arrangement is intended for use of the device as a 5-channel first-level and one-channel second-level multiplexer. Each of the six gates are provided with an internal „pull-up" current which may be turned ON or OFF by connecting the pull-up control terminal (P) to a negetive supply or to the body (B) terminal.

FEATURES

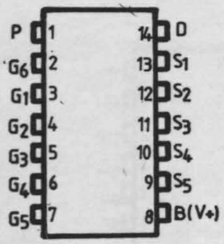
- Drain-source ON resistance 100 ohms
- Maximum switched voltage ±30V
- Maximum voltage in each terminal to, substrate −30 V
- All inputs protected

ABSOLUTE MAXIMUM RATINGS

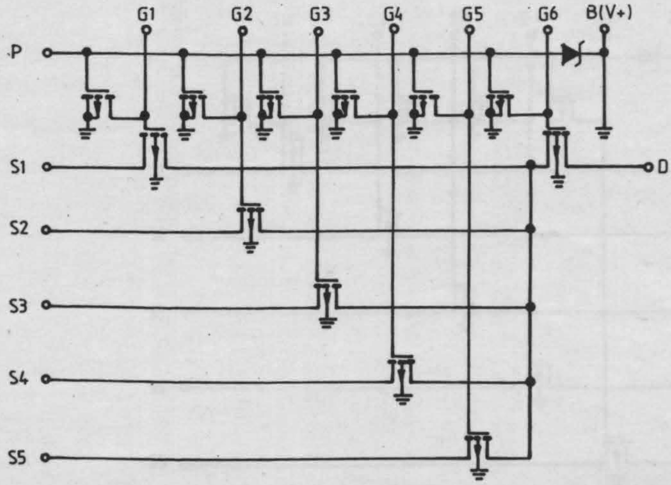
Bulk to source voltage	V_{BS}	−2to +30 +30	V
Bulk to drain voltage	V_{BD}	+30	V
Drain to source voltage	V_{DS}	±30	V
Bulk to gate voltage	V_{BG}	+35	V
Bulk to P terminal voltage	V_{BP}	+35	V
Drain, source current	I_D, I_S	100	mA
Power disipation	P_d	600	mW*
		900	mW
Storage temperature	T_{stg}	−55°C to 150 °C	
Operating temperature	T_A	0°C to 70 °C	

* for ceramic package

PIN CONNECTIONS



SCHEMATIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

PARAMETER		TEST CONDITIONS	VALUES min.	VALUES typ.	VALUES max.	UNIT
V_T	Threshold voltage	$I_D = -10\ \mu A$, $V_{SB} = V_{DG} = 0\ V$	−1.5		−4	V
BV_{DS}	Drain-source breakdown voltage	$I_D = -50\ \mu A$, $V_{GS} = V_{SB} = 0\ V$	−30			V
BV_{SD}	Source-drain breakdown voltage	$I_S = -10\ \mu A$, $V_{GD} = 0\ V$	−30			V
BV_{GB}	Gate-bulk breakdown voltage	$I_G = -10\ \mu A$,	−30			V
BV_{PB}	P terminal-bulk breakdown voltage	$I_P = -10\ \mu A$, $V_{GB} = 0\ V$	−30			V
r_{ON}	Drain-source on resistance	$I_S = -1\ mA$, $V_{DB} = 0\ V$ $V_{GD} = -30\ V$			125	Ω
		$I_S = -1 mA$, $V_{DB} = -10\ V$, $V_{GD} = -20\ V$			200	Ω
		$I_S = -1 mA$, $V_{DB} = -20\ V$ $V_{GD} = -10\ V$			650	Ω
$I_{S(OFF)}$	Source off leakage current	$V_{SD} = -20\ V$, $V_{GD} = 0\ V$			−5	nA
$I_{D(OFF)}$	Drain off leakage current	$V_{DS} = -20\ V$, $V_{GS} = 0\ V = V_{SB}$			−25	nA
$I_{G(ON)}$	Gate on current	$V_{GB} = -30\ V$, $V_{PB} = -30\ V$	−0.8		−3.4	mA
I_{GSS}	Gate-channel leakage current	$V_{GB} = -20\ V$			−5	nA

* $V_{DB} = 0\ V$, $V_{PB} = 0\ V$, unless otherwise specified

3x2–CHANNEL ANALOG SWITCHES

GENERAL DESCRIPTION

The MMP 119 contains six enhancement-mode P-channel MOS FETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltage up to 30 V peak-to-peak. The switches are integrated onto a silicon substrate (body) and are internally connected into two groups of three switches per group. This arrangement facilitates the switching or multiplexing of differential analog signals. Each group has a common drain terminal (D_1 and D_2) which will function equally well as a common source. Each gate terminal (G) controls a pair of switches and is provided with a normally-OFF „pull-up" MOS FET which may be turned ON to provide a current source to the gate-driving circuit. The pull-ups are turned ON or OFF by connecting the „P" terminal to a negative supply or to the „B" terminal respectively.

FEATURES

- Drain-source ON resistance 100 ohms
- Maximum switched voltage ±30V
- Maximum voltage in each terminal to, substrate −30 V
- All inputs protected

APPLICATIONS

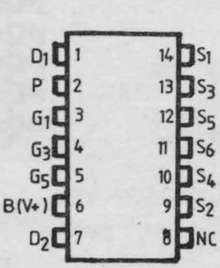
- Switching analog signals such as differential inputs
- Multiplexing

ABSOLUTE MAXIMUM RATINGS

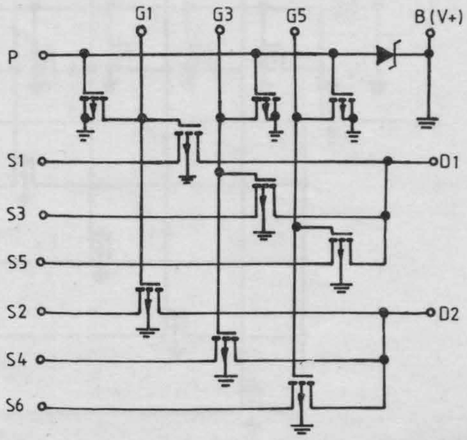
Bulk to source voltage	V_{BS}	+30 V
Bulk to drain voltage	V_{BD}	+30 V
Drain to source voltage	V_{DS}	±30 V
Bulk to gate voltage	V_{BG}	+35 V
Bulk to P terminal voltage	V_{BP}	+35 V
Drain, source current	I_D, I_S	100 mA
Power disipation	P_d	600 mW*
		900 mW
Storage temperature	T_{stg}	−55°C to 150 °C
Operating temperature	T_A	0°C to 70 °C

* for ceramic package

PIN CONNECTIONS



SCHEMATIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS $T_A = -25°C$

PARAMETER		TEST CONDITIONS	VALUES			UNIT
			min.	typ.	max.	
V_T	Threshold voltage	$I_D = -10\ \mu A,\ V_{SB} = V_{DG} = 0\ V$	−1.5		−4	V
BV_{DS}	Drain-source breakdown voltage	$I_D = -50\ \mu A,\ V_{GS} = V_{SB} = 0\ V$	−30			V
BV_{SD}	Source-drain breakdown voltage	$I_S = -10\ \mu A,\ V_{GD} = 0\ V$	−30			V
BV_{GB}	Gate-bulk breakdown voltage	$I_G = -10\ \mu A,$	−30			V
BV_{PB}	P terminal-bulk breakdown voltage	$I_P = -10\ \mu A,\ V_{GB} = 0\ V$	−30			V
r_{ON}	Drain-source on resistance	$I_S = -1\ mA,\ V_{DB} = 0\ V$ $V_{GD} = -30\ V$			125	Ω
		$I_S = -1 mA,\ V_{DB} = -10\ V,$ $V_{GD} = -20\ V$			200	Ω
		$I_S = -1 mA,\ V_{DB} = -20\ V$ $V_{GD} = -10\ V$			650	Ω
$I_{S(OFF)}$	Source off leakage current	$V_{SD} = -20\ V,\ V_{GD} = 0\ V$			−5	nA
$I_{D(OFF)}$	Drain off leakage current	$V_{DS} = -20\ V,\ V_{GS} = 0\ V = V_{SB}$			−25	nA
$I_{G(ON)}$	Gate on current	$V_{GB} = -30\ V,\ V_{PB} = -30\ V$	−0.8		−3.4	mA
I_{GSS}	Gate-channel leakage current	$V_{GB} = -20\ V$			−5	nA

* $V_{DB} = 0\ V,\ V_{PB} = 0\ V$, unless otherwise specified

2x2–CHANNEL ANALOG SWITCH

GENERAL DESCRIPTION

The MMP 122 contains four enhancement-mode P-channel MOS FETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 30 V peak-to-peak. The switches are integrated onto a silicon substrate (body) and are internally connected into two groups of two switches per group. This arrangement facilitates the switching or multiplexing of differential analog signals. Each group has a common drain terminal (D_1 and D_2) which will function equally well as a common source. Each gate terminal (G) controls a pair of switches and is provided with a normally-OFF "pull-up" MOS FET which may be turned ON to provide a current source to a gate-driving circuit. The pull-ups are turned ON or OFF by connecting the "P" terminal to a negative supply or to the "B" terminal respectively.

FEATURES

- Drain-source ON resistance 100 ohms
- Maximum switched voltage ±30V
- Maximum voltage in each terminal to, substrate −30 V
- All inputs protected

APPLICATIONS

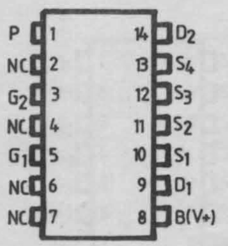
- Switching analog signals such as differential inpuls
- Multiplexing

ABSOLUTE MAXIMUM RATINGS

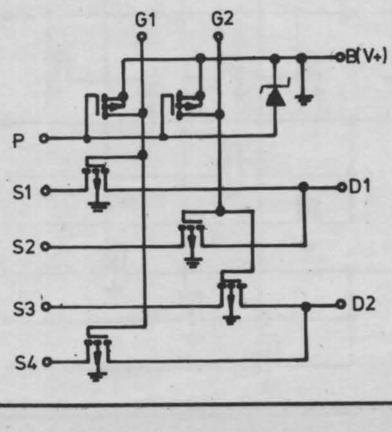
Bulk to source voltage	V_{BS}	+30 V
Bulk to drain voltage	V_{BD}	+30 V
Drain to source voltage	V_{DS}	±30 V
Bulk to gate voltage	V_{BG}	+35 V
Bulk to P terminal voltage	V_{BP}	+35 V
Drain, source current	I_D, I_S	100 mA
Power disipation	P_d	600 mW*
		900 mW
Storage temperature	T_{stg}	−55°C to 150 °C
Operating temperature	T_A	0°C to 70 °C

* for ceramic package

CONNECTION DIAGRAM



SCHEMATIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS $T_A = 25°C$

PARAMETER		TEST CONDITIONS	VALUES			UNIT
			min.	typ.	max.	
V_T	Threshold voltage	$I_D = -10\ \mu A,\ V_{SB} = V_{DG} = 0\ V$	−1.5		−4	V
BV_{DS}	Drain-source breakdown voltage	$I_D = -50\ \mu A,\ V_{GS} = V_{SB} = 0\ V$	−30			V
BV_{SD}	Source-drain breakdown voltage	$I_S = -10\ \mu A,\ V_{GD} = 0\ V$	−30			V
BV_{GB}	Gate-bulk breakdown voltage	$I_G = -10\ \mu A,$	−30			V
BV_{PB}	P terminal-bulk breakdown voltage	$I_P = -10\ \mu A,\ V_{GB} = 0\ V$	−30			V
r_{ON}	Drain-source on resistance	$I_S = -1\ mA,\ V_{DB} = 0\ V$ $V_{GD} = -30\ V$			125	Ω
		$I_S = -1 mA,\ V_{DB} = -10\ V,$ $V_{GD} = -20\ V$			200	Ω
		$I_S = -1 mA,\ V_{DB} = -20\ V$ $V_{GD} = -10\ V$			650	Ω
$I_{S(OFF)}$	Source off leakage current	$V_{SD} = -20\ V,\ V_{GD} = 0\ V$			−5	nA
$I_{D(OFF)}$	Drain off leakage current	$V_{DS} = -20\ V,\ V_{GS} = 0\ V = V_{SB}$			−25	nA
$I_{G(ON)}$	Gate on current	$V_{GB} = -30\ V,\ V_{PB} = -30\ V$	−0.8		−3.4	mA
I_{GSS}	Gate-channel leakage current	$V_{GB} = -20\ V$			−5	nA

* $V_{DB} = 0\ V,\ V_{PB} = 0\ V$, unless otherwise specified

4-CHANNEL ANALOG SWITCH

GENERAL DESCRIPTION

The MMP 124 contains four enhancement-mode P-channel MOS FETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 30 V peak-to-peak. The switches are integrated on a silicon substrate (body). The switches have a common drain terminal (D) which will function equally well as a common source. In the same manner, the source terminals (S) will function equally well as drains. Each gate (G) is provided with a normally-OFF „pull-up" MOS FET which may be turned ON to provide a current source to a gate-driving circuit. The pull-ups are turned ON or OFF by connecting the „P" terminal to a negative supply or to the „B" terminal respectively.

FEATURES

- Drain-source ON resistance 100 Ωs
- Maximum switched voltage ± 30 V
- Maximum voltage in each terminal to substrate −30 V
- All inputs protected

APPLICATIONS

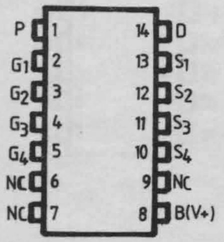
- Switching analog signals
- Multiplexing

ABSOLUTE MAXIMUM RATINGS

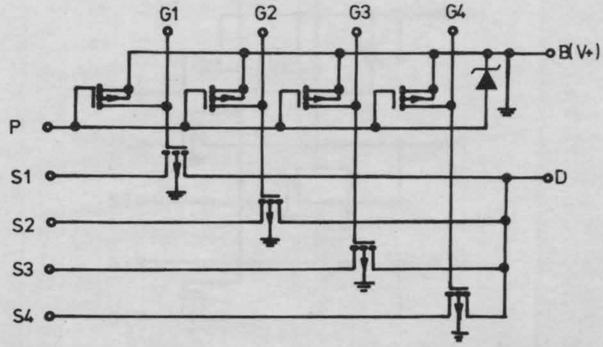
Bulk to source voltage	V_{BS}	+ 30 V
Bulk to drain voltage	V_{BD}	+ 30 V
Drain to source voltage	V_{DS}	± 30 V
Bulk to gate voltage	V_{BG}	+ 35 V
Bulk to P terminal voltage	V_{BP}	+ 35 V
Drain, source current	I_D, I_S	100 mA
Power disipation	P_d	600 mW 900 mW※
Storage temperature	T_{stg}	−55°C to 150°C
Operating temperature	T_t	0°C to 70°C

※ for ceramic package

PIN CONNECTIONS



SCHEMATIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS $T_A = 25°C$

PARAMETER		TEST CONDITIONS	VALUES			UNIT
			min.	typ.	max.	
V_T	Threshold voltage	$I_D = -10\ \mu A$, $V_{SB} = V_{DG} = 0\ V$	−1.5		−4	V
BV_{DS}	Drain-source breakdown voltage	$I_D = -50\ \mu A$, $V_{GS} = V_{SB} = 0\ V$	−30			V
BV_{SD}	Source-drain breakdown voltage	$I_S = -10\ \mu A$, $V_{GD} = 0\ V$	−30			V
BV_{GB}	Gate-bulk breakdown voltage	$I_G = -10\ \mu A$,	−30			V
BV_{PB}	P terminal-bulk breakdown voltage	$I_P = -10\ \mu A$, $V_{GB} = 0\ V$	−30			V
r_{ON}	Drain-source on resistance	$I_S = -1\ mA$, $V_{DB} = 0\ V$ $V_{GD} = -30\ V$			125	Ω
		$I_S = -1\ mA$, $V_{DB} = -10\ V$, $V_{GD} = -20\ V$			200	Ω
		$I_S = -1\ mA$, $V_{DB} = -20\ V$ $V_{GD} = -10\ V$			650	Ω
$I_{S(OFF)}$	Source off leakage current	$V_{SD} = -20\ V$, $V_{GD} = 0\ V$			−5	nA
$I_{D(OFF)}$	Drain off leakage current	$V_{DS} = -20\ V$, $V_{GS} = 0\ V = V_{SB}$			−25	nA
$I_{G(ON)}$	Gate on current	$V_{GB} = -30\ V$, $V_{PB} = -30\ V$	−0.8		−3.4	mA
I_{GSS}	Gate-channel leakage current	$V_{GB} = -20\ V$			−5	nA

* $V_{DB} = 0\ V$, $V_{PB} = 0\ V$, unless otherwise specified

1000: 1 STATIC FREQUENCY DIVIDER

GENERAL DESCRIPTION

The MMP 131 types are 1000:1 static frequency dividers integrated circuits fabricated In standard PMOS aluminium-gate technology. The circuit contains 11 Master-Slave Flip-Flops and a preseting logic. The first 10 Flip-Flops are dividing the frequency and the 11th is for the generation of the output pulse.
The circuit is available either with the preset internally connected or with external preset. The MMP 131 types are supplied in 4-lead (TO-72) or 8 — lead (TO-99) metal case and 8-lead dual-in-line plastic package (MP-48)

FEATURES

- One supply voltage only (max V_{DD} = −20 V)
- Low power consumption
- Maximum input signal frequency 25 kHz

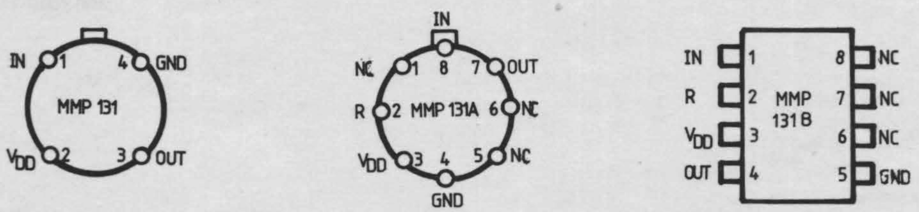
APPLICATIONS

- Frequency divider
- Relays
- Switches with time delay

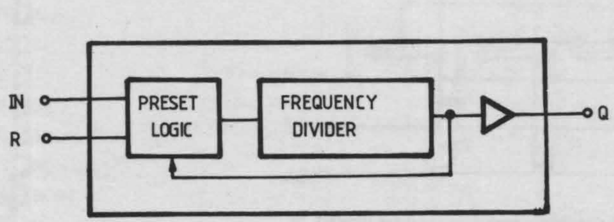
ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	−24 to +0,3 V
V_I	Voltage between any pin and ground	−24 to +0,3 V
I_O	Output current	−2 mA
T_A	Operating temperature	0 to 70 °C
T_{stg}	Storage temperature	−33 to +125 °C

PIN CONNECTIONS



BLOCK DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, unless otherwise specified)

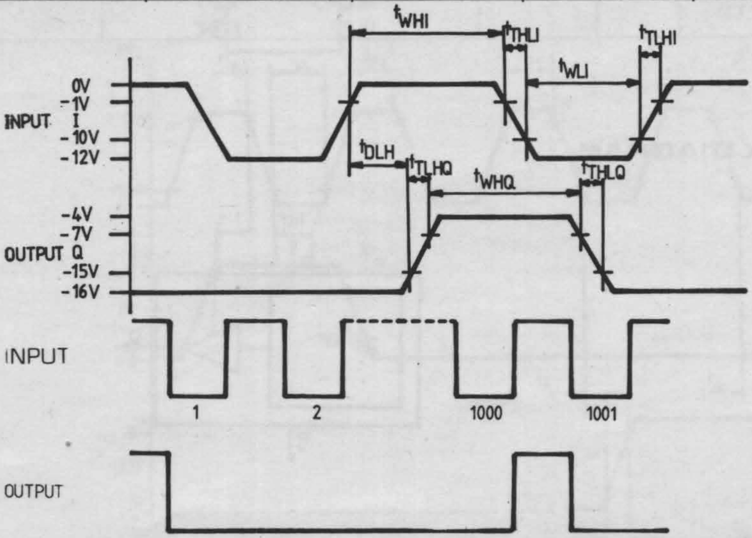
PARAMETER		CONDITIONS $V_{DD} = -19$ V	VALUES min	VALUES max.	UNIT
V_{DD}	Supply voltage		−20	−18	V
I_{DD}	Supply current		−4		V
V_{IH}	Input high voltage		−2		V
V_{IL}	Input low voltage			−12	V
R_I	Input resistance		10		MΩ
V_{OH}	Output high voltage	$I_O = -1$ mA	−7		V
V_{OL}	Output low voltage			−15	V
I_{OH}	Output drive current	$R_L = 10$ kΩ		−1	mA
I_{OL}	Output sink current	$R_L = 10$ kΩ	−10		μA

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, unless otherwise specified)

PARAMETER		CONDITIONS $V_{DD} = -19$ V	VALUES min.	VALUES max.	UNIT
Input signal					
f_I	Input signal frequency		0	25	kHz
t_{WL}	Low voltage pulse width		10		μs
t_{WH}	High voltage pulse width		15		μs
t_{THL}, t_{TLH}	Input rise and fall times			2	μs
Output signal					
t_{WH}	High voltage pulse width		5		μs
t_{PLH}	Propagation delay time			15	μs
t_{TLH}	Output rise times			5	μs
t_{THL}	Output fall time			10	μs
Preset signal					
t_{WL}	Low voltage pulse width		10		μs
t_{THL}, t_{TLH}	Preset rise and fall times			2	μs

TIMING DIAGRAM



256-BIT DYNAMIC SHIFT REGISTER

GENERAL DESCRIPTION

The MMP 156 contains one 256-bit shift register with one serial input and one serial output. It dissipates very little power and uses a one-phase external clock. The device has a low impedance push-pull output buffer which, when appropriately biased is capable of interfacing direct with MOS, DTL, TTL and other loads.
The buffer supply terminal P_2 is a separate supply which determines the output LOW signal only. This provides an output level that is independent of both the amplitude and width of the clock pulse. The MMP 156 is a MOS standard aluminium gate technology, available in 14 lead dual-in-line package.

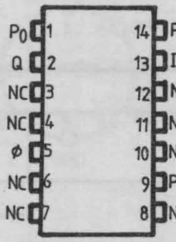
FEATURES

- Single clock signal
- 1 MHz operation guaranteed
- Low power consumption

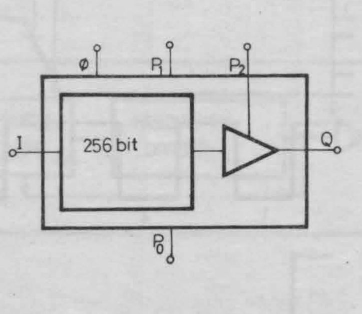
ABSOLUTE MAXIMUM RATINGS

	Voltages on all data inputs, clock inputs and supply terminals with reference to P_0	−30 to +0,3 V
P_{tot}	Power dissipation	500 mW
T_A	Operating temperature	0 to 70 °C
T_{stg}	Storage temperature	−33 to 125 °C

PIN CONNECTIONS



BLOCK DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

($V_{P1} = -26$ to -28 V, $V_{P2} = -12$ to -14 V, $T_A = 25°C$, P_O = grounded, standard load of 20 kΩ in parallel with 50 pF to P_O)

PARAMETER		TEST CONDITIONS	VALUES min.	VALUES typ.	VALUES max.	UNIT
V_{P1}	Supply voltages		−28	−26	−24	V
V_{P2}			−14	−13	−12	V
$V_{\varnothing H}$	Clock pulse high voltage		−2		+0,3	V
$V_{\varnothing L}$	Clock pulse low voltage		−28	−12	−9	V
V_{IH}	Input high voltage		−2		+0,3	V
V_{IL}	Input low voltage		−28	−12	−9	V
V_{QH}	Output high voltage		−0,5		0	V
V_{QL}	Output low voltage		−14		−10	V
R_{QH}	Output high resistance				500	Ω
R_{QL}	Output low resistance				500	Ω
$-I_{P1}$	Power supply current				10	mA

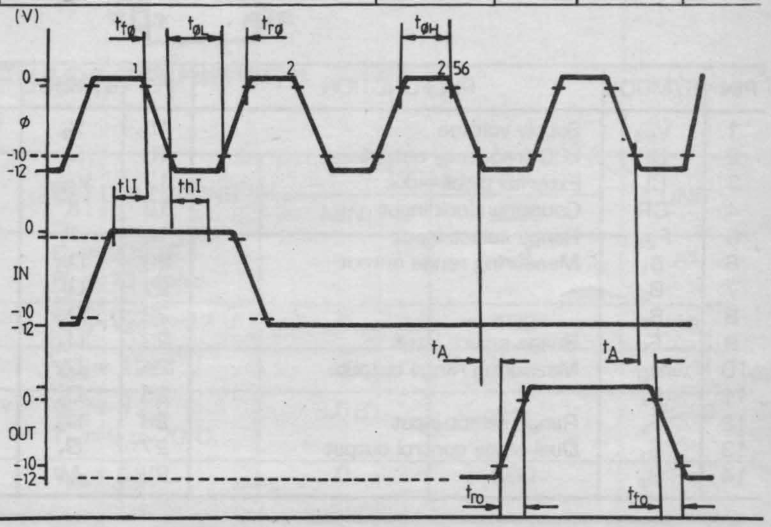
NOTES: 1. The output buffer power supply current I_{P2} is almost entirely dependent on the external load.
2. The active level voltage is the low voltage level.

DINAMIC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$

PARAMETER		TEST CONDITIONS	VALUES min.	VALUES typ.	VALUES max.	UNIT
$f_{\varnothing}$	Clock rate					
	MMP 156		0,01		1	MHz
	MMP 156-1		0,01		0,8	MHz
$t_{\varnothing L}$	Clock pulse width					
	MMP 156		0,5		50	μs
	MMP 156-1		0,6		50	μs
$t_{r\varnothing}$	Clock pulse rise time				100	ns
$t_{f\varnothing}$	Clock pulse fall time				100	ns
t_{ll}	Data lead time		100			ns
t_{hl}	Data hold time		100			ns
T_{rO} t_{fO}	Output rise and fall time				150	ns
t_A	Delay time				400	ns

TIMING DIAGRAM



DIGITAL MULTIMETER LOGIC

GENERAL DESCRIPTION

MMP 190 is a digital multimeter logic integrated circuit fabricated in PMOS enhancement-depletion aluminium gate technology. The circuit consists of 2 internal oscilators (one for multiplexing, one for counting), a 4 decades BCD counter, an output multiplexer which can drive a LED or LCD 3 3/4 digit display and an autoranging and dual-slope A/D conversion control logic.
MMP 190 is supplied in 28-lead dual-in-line plastic packages.

FEATURES

- 3 3/4 digit digital multimeter logic (max. 599.9)
- autoranging
- multiplexed BCD output
- dual-slope integration
- overrange indicated (blinking)
- low-power dissipation
- CMOS compatibility

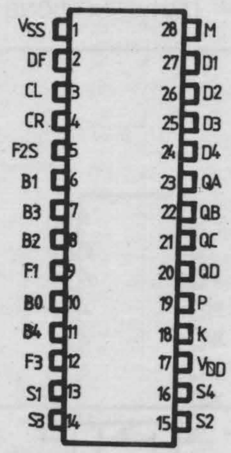
APPLICATIONS

- digital multimeter
- decade counter

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	-20 to +0.3	V
V_I	Voltage between any pin and ground	-20 to +0.3	V
I_F	Input current ($V_I = 0.3$ V; $V_{SS} = 0$ V)	1	mA
T_A	Operating ambient temperature	0 to +70	°C
T_{stg}	Storage temperature	-55 to +125	°C

PIN CONNECTIONS



PIN	SYMBOL	PIN FUNCTION	PIN	SYMBOL	PIN FUNCTION
1	V_{SS}	Supply voltage	15	S_2	Dual-slope control output
2	DF	LCD frequency output	16	S_4	"
3	CL	External clock input	17	V_{DD}	Supply voltage
4	CR	Counting clock input	18	K	Analog input
5	F_{2S}	Range select input	19	P	Polarity output
6	B_1	Measuring range output	20	Q_D	BCD output
7	B_3	"	21	Q_C	"
8	B_2	"	22	Q_B	"
9	F_1	Range select input	23	Q_A	"
10	B_0	Measuring range output	24	D_4	Digit selection output
11	B_4	"	25	D_3	"
12	F_3	Range select input	26	D_2	"
13	S_1	Dual-slope control output	27	D_1	"
14	S_3	"	28	M	Scan oscilator input

STATIC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$, unless otherwise specified)

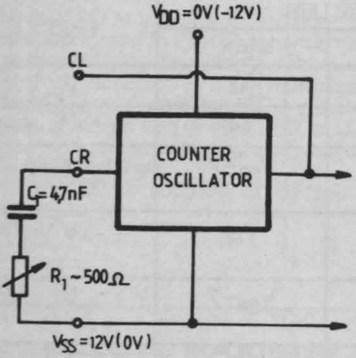
	PARAMETER	TEST CONDITIONS	VALUES MIN.	VALUES MAX.	UNIT
V_{DD}	Supply voltage	reference	0	0	V
V_{SS}	Supply voltage	$V_{DD} = 0$ V	8	14	V
V_{IL}	K input low voltage	$V_{DD} = 0$ V $f_N = 30$ kHz	0	$V_{SS}-7$	V
V_{IH}	K input high voltage	$V_{DD} = 0$ V $f_N = 30$ kHz	$V_{SS}-2$	V_{SS}	V
V_{IL}	Input low voltage (except K input)	$V_{DD} = 0$ V $f_N = 30$ kHz	0	$V_{SS}-7$	V
V_{IH}	Input high voltage (except K input)	$V_{DD} = 0$ V $f_N = 30$ kHz	$V_{SS}-0.5$	V_{SS}	V
V_{OL}	Output low voltage (Q_A, Q_B, Q_C, Q_D, D_1, D_2, D_3, D_4, P outputs)	$I_O = 25\ \mu A$	0	1	V
V_{OH}	Output high voltage (Q_A, Q_B, Q_C, Q_D, D_1, D_2, D_3, D_4, P outputs)	$I_O = -200\ \mu A$	$V_{SS}-1$	V_{SS}	V
V_{OL}	Output low voltage (B_0, B_1, B_2, B_3,B_4, S_1, S_2, S_3, S_4 outputs)	$I_O = 50\ \mu A$	0	1	V
V_{OH}	Output high voltage (B_0, B_1, B_2, B_3, B_4, S_1, S_2, S_3, S_4 outputs)	$I_O = -200\ \mu A$	$V_{SS}-1$	V_{SS}	V
V_{OL}	DF output low voltage	$I_O = 50\ \mu A$	0	1	V
V_{OH}	DF output high voltage	$I_O = -50\ \mu A$	$V_{SS}-1$	V_{SS}	V
P_d	Power dissipation	$V_{DD}-V_{SS} = 12$ V open outputs		70	mW

DYNAMIC ELECTRICAL CHARACTERISTICS

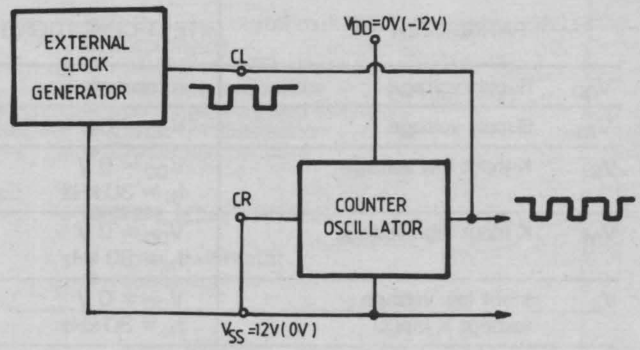
($T_A = 25°C$, unless otherwise specified)

	PARAMETER	TEST CONDITIONS	VALUES MIN.	VALUES MAX.	UNIT
t_d	Delay time between K input and S outputs	$C_L = 200$ pF $R_L = 10$ Mohm		4	μs
f_N	Counter oscilator frequency	$V_{DD}-V_{SS} = -12$ V	0	100	kHz
$F_{N(V)}$	Counting frequency stability	$V_{SS} = 12 \pm 1$ V	±3		%/V
$F_{N(T)}$	Counting frequency stability	$V_{SS} = 12$ V $T_O = 0$ to 70°C	±0.8		%/°C
f_M	Multiplexing frequency	$V_{SS} = 12$ V	0	800	Hz

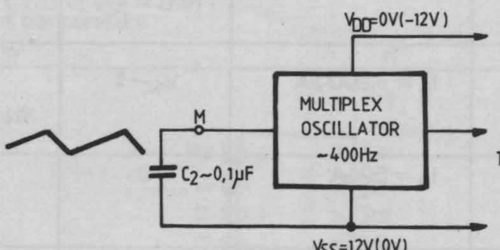
MODES OF OPERATION

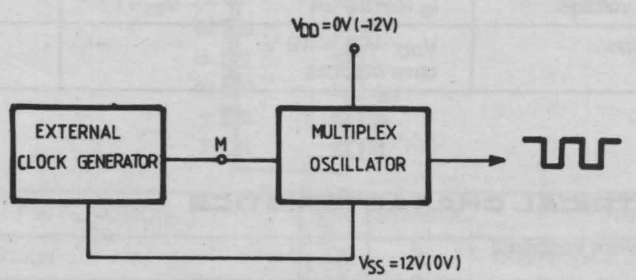


* Input CL open



* Input CR connected to V_{SS}





* Only for testing purposes and R_l 0

FUNCTIONAL DESCRIPTION

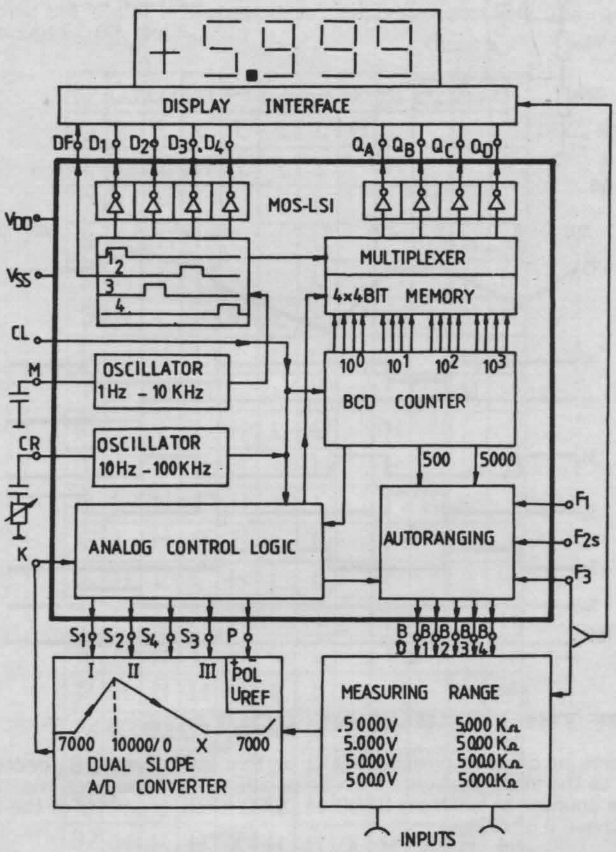
GENERAL

The circuit comprises the logic functions for a digital multimeter, on the basis of dual-slope method, with automatic range switching. By means of four measuring-range outputs, small units with 3 3/4 digits and four measuring ranges can be realized without additional external components for the range selection. By switching the logic range, up to eight different measuring ranges can be switched automatically; however, decoding of these ranges must be done externally.
The maximum display is 6000. 6000 steps mean a relatively small analog circuit requirement, however, that permit the measuring of voltages between 100 μA and 600 V in four measuring ranges. When the highest measuring range is exceeded, the value 6000 is displayed. Through an additional blinking circuit, which does nót require an additional connection pin, the user is made aware of the measuring range being exceeded.

FUNCTION

The block diagram shows a simple unit with four automatically selected measuring ranges. The external analog portion consists of only the analog amplifiers, reference voltage source, and the analog switches for the measuring phase and range switching.

BLOCK DIAGRAM

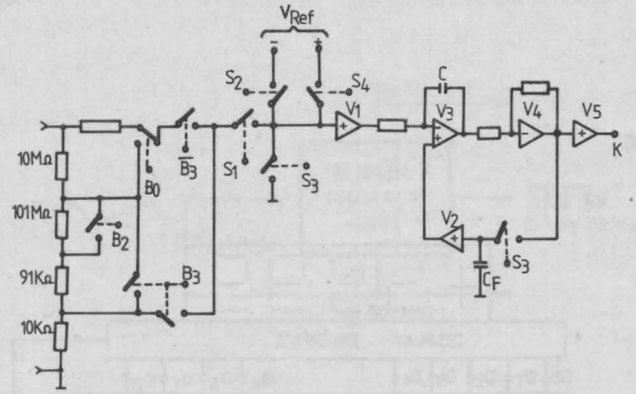


The sequence control and generation of the value measured is done by the MMP 190. The main portion of the circuit is made up of a four decade BCD counter which is driven by a counting oscillator contained on the chip, together with an externally connected RC-circuit. The counting oscillator may be replaced by connecting a clock generator. At particular periods of timing, the contents of the counter is transferred into the 4 x 4-bit memory by means of a strobe pulse derived from the K-input.
The information contained in the memory is transfered by means of a multiplexer in a bit-parallel mode to outputs Q_A through Q_D, whereby outputs D_1 through D_4 indicate the just transferred decimal place ($Q_A \triangleq$ LSB, $Q_D \triangleq$ MSB; $D_1 \triangleq$ units digit, $D_4 \triangleq$ thousands digit, active condition = high level). To ensure reliable driving of the memories in the display interface, e.g. liquid crystal display, the correct BCD-information is maintained at the Q outputs until after the end of the active condition of the D-outputs. The indication of the decimal position occcurs in the sequence 1-3-2-4, to avoid flickering when the display units are driven directly.
For the generation of scan-frequency for the multiplexer a second oscillator has been provided on the MMP 190. Replacement by an external clock generator is possible but should be used only for testing purposes. The display frequency DF of about 50 Hz required by liquid crystal displays is also derived from the multiplex oscillator.

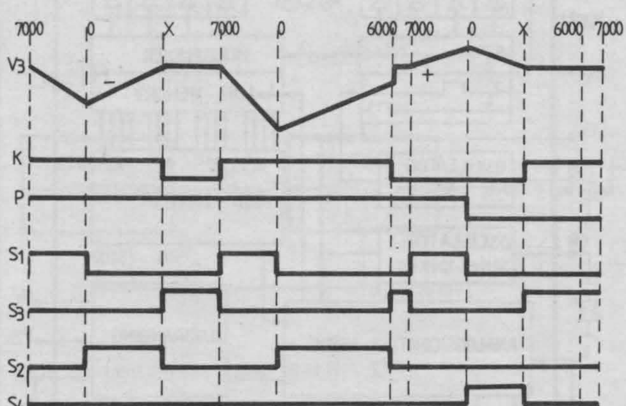
MEASURING SEQUENCE

The measuring sequence is also controlled by the BCD-counter, via measuring-phase outputs S_1 through S_4 (compare timing diagram and principle circuit diagram).

EXTERNAL ANALOG CIRCUIT



TIMING DIAGRAM



PHASE I, INTEGRATION OF THE MEASURING VOLTAGE

The measuring cycle starts at counter position 7000; at this point output S_1 becomes high, whereby the input voltage is switched to the integrator until counter position 0000 has been reached.
At the moment when the counter jumps from 9999 to 0000, the signal level of the comparator (input k) is stored. At this moment phase II is started.

PHASE II, INTEGRATION OF REFERENCE VOLTAGE

Depending on the condition of the comparator, only S_2 or S_4 is activated whereby the reference voltage is switched to the integrator with a polarity opposite to the previously applied input voltage. With this reference voltage the integrator is reduced until the sensitivity threshold of the comparator has been reached and the signal condition at the input K changes. This change of signal activates S_3. The number of counting pulses between counter position 0000 and X is proportional to the measuring voltage. Through the low-high transition of S_3 the counter contents is loaded into the display memory; at this point of time phase III is started.

PHASE III, ZERO REGULATION

In this process the input of the AD-converter is set to zero and the resulting error voltage is stored in capacitor C_F. An error voltage is compensated by a feedback loop. The duration of phase I is determined by the counter frequency and the fixed number of 3000 counting steps. For a 30 KHz counting frequency, phase I lasts exactly 100 ms. The longer the integration time, the better the suppression of noise voltages superimposed on the measuring signal. If the duration of the noise voltage period is contained in the integration time as an even number, this noise is suppressed completely. As noise voltages can be expected to occur especially at line frequency, 100 ms integration time constitute a favourable compromise between integration time and noise voltage suppression. The duration of phase II is determined by the level of the measuring voltage. If the measuring voltage is too large, the integrator cannot be discharged during the 6000 counting steps available as a maximum; consequently, at step 6000 phase III is initiated. Hence. the integrator will have assumed the correct starting position at the begining of phase I which follows.
For excessive measuring voltages the display is therefore 6000. In order to bring the incorrectness of this display to the user's attention, the pseudo-decade HHHH is made active at the outputs, synchronously to signal S_1; thereby a blinking effect of approx. 3 Hz is obtained.

AUTOMATIC RANGE SWITCHING

The measuring range is changed whenever the measuring result has been $\geqslant 5500$ or < 500. For $n \geqslant 5500$ the range counter (3 bit up/down counter) is stepped by one count, for $n < 500$ stepped down by one, whereby the counter is blocked on the lowest or highest digit position, respectively. The range selection can be controlled through control inputs F_1, F_{2S} and F_3.

TRUTH TABLE

Nr	Q3	Q2	Q1	F1	F2S	F3	B0	B1	B2	B3	B4
0	L	L	L	L	L	L	H				
1	L	L	H	L	L	L		H			
2	L	H	L	L	L	L			H		
3	L	H	H	L	L	L				H	
4	H	L	L	L	L	L				H	H
5	H	L	H	L	L	L				H	H
6	H	H	L	L	L	L				H	H
7	H	H	H	L	L	L				H	H
10	L	L	L	H	L	L		H			
11	L	L	H	H	L	L		H			
12	L	H	L	H	L	L			H		
13	L	H	H	H	L	L				H	
14	H	L	L	H	L	L					H
15	H	L	H	H	L	L					H
16	H	H	L	H	L	L					H
17	H	H	H	H	L	L					H
2X	Q3	Q2	Q1	X	H	L	X	Q1	X	Q2	Q3
30	H	H	H	L	L	H				H	H
31	H	H	H	H	L	H					H
32	H	H	H	X	H	H	X	H	X	H	H

When the control inputs F_1, F_{2S} and F_3 are in a low condition, the counter can move within the lower 5 positions up or down. Should it be in a higher position, it can step only downward until the "free zone" has been reached; the decoder produces correct values also for counter positions outsside the "free zone" so that the system adjusts itself.
By an H-signal at input F_1 the correlation between the counter position and decoder output can be changed. Thereby it is made possible to perform range setting for the voltage and resistance ranges and the control of the decimal point in a simple unit with four measuring ranges without external decoding. Input F_3 is used to set the counter to the highest level. The highest measuring range is activated and maintained as long as F_2 is kept at a high level. For example, thereby the range 500.0V is activated, which is an advantage for quick overview-measurements.
A high level at input F_{2S} has the effect that the outputs of the range counter are directly transferred to the outputs 8 different ranges are then available which must be decoded by external means. In the case of F_{2S} = H, the "frea zone" of the counter is expanded to the full counting range; the prevention of "running wild" is maintained.

THE TRUTH TABLE FOR SETTING THE MEASURING RANGES SHOULD BE UNDERSTOOD AS FOLLOWS:

The range outputs B_0...B_4 are intended to directly drive the five possible decimal places of a 4 decade display. Simple units with 4 measuring ranges have been taken into consideration. For example, in the case of voltages the measuring ranges with F_1 = low are:

B_0	.5000 V
B_1	5.000 V
B_2	50.00 V
B_3	500.0 V

The total measuring range therefore comprises 0.1 mV through 599.9 V. For resistance measuring, however, F_1 must be high:

B_1	5.000 kohm
B_2	50.00 kohm
B_3	500.0 kohm
B_4	5000. kohm

The total measuring therefore comprises 1 ohm through 5.999 Mohm. Hence, using control input F_1, a choice of one of the two groups is basically possible.
The range outputs are also intended to directly drive the appropriate four selection relays without additional logic gating. When the automatic range selection (e.g. after turn-on) has not yet found the correct range, some measuring range expected to be shown anyway. This side-condition is considered in the truth table of vectors 0...17.
It should be noted, however, that Q_1, Q_2, and Q_3 in the truth table are internal outputs of the built-in up-down counter. It is also possible to select one of 5 measuring ranges automatically. To do this, the 4th and the 5th measuring ranges are separated by external gating at F_1 = low (whereby $MB_4 = B_3$; $\overline{B}_4$ and $MB_5 = B_4$). MB_4 is measuring range 4, MB_5 is measuring range 5.
F_{2S} = high causes an extension of all eight possible measuring ranges. The range selected appears at outputs B_1 (=Q_1), B_3 (=Q_2), and B_4 (=Q_3) dual-coded. Hence, vectors 20...27 of the truth table are fixed.

5-STAGE STATIC SHIFT REGISTER SYNCHRONOUS PARALLEL OR SERIAL INPUT/PARALLEL OUTPUT

GENERAL DESCRIPTION

MMP 311 contains one 5-stage shift register synchronous parallel or serial input/parallel output, having two external clocks, a single serial data input, a parallel control input and individual parallel inputs to each register stage.
Each register stage is a quasi-static D-type master-slave flip-flop. When Ø1 is static on "HIGH" and Ø2 is "LOW" each stage becomes a static memory cell, and the logic level present at each data input I_i is immediately transferred to the data output O_i. When the two external clocks are applied, and the parallel control input, I_p is "HIGH" data is serially shifted into the 5-stage register, from I_s to O_i. When $I_p \cdot Ø2 =$ "LOW" and Ø1 = "HIGH" data is jammed into the 5-stage register and remains unaffected as long as Ø1 is "HIGH". Data is serially shifted with the negative transition of the Ø1 clock line.

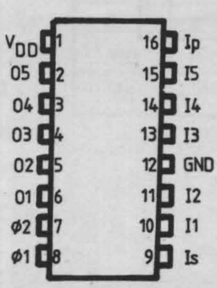
ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	−31...0.3	V
$V_Ø$	Clock input voltage	−31...0.3	V
V_i	Data input voltage	−25...+0.3	V
T_{op}	Operating temperature	0...70	°C
T_{ST}	Storage temperature	−55...+85	°C

RECOMANDED OPERATING CONDITIONS

V_{DD}	Supply voltage	−13 ± 0.5	V
$V_Ø$	Clock voltage	−26 ± 2	V

PIN CONNECTIONS



STATIC ELECTRICAL CHARACTERISTICS •

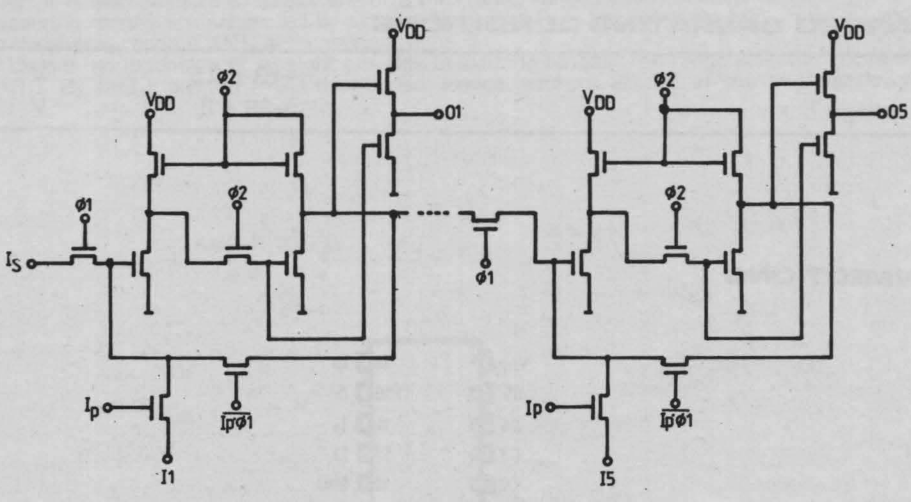
	PARAMETER	TEST CONDITIONS	VALUES			UNIT
			min.	typ.	max.	
I_{LI}	data input quiescent current	$V_I = -25$ V			10	μA
$I_{L\varnothing 1}$	clock input quiescent current	$V_I = -31$ V			50	μA
$I_{L\varnothing 2}$	clock input quiescent current	$V_I = -31$ V			1	mA
V_{OL}	output low voltage	$V_{IH} \geq -2$ V $V_{IL} \leq -9$ V $R_L = 100$ K			−10	V
V_{OH}	output high voltage	$V_{IH} \geq -2$ V $V_{IL} \leq -9$ V	−1			V
V_{OL}	output low voltage	$I_O = 1$ mA $V_{IH} \geq -2$ V $V_{IL} \leq -9$ V			−5	V
$V_{\varnothing H}$	output high voltage	$I_O = -1$ mA $V_{IH} \geq -2$ V $V_{IL} \leq -9$ V	−3			V

DYNAMIC ELECTRICAL CHARACTERISTICS •

	PARAMETER	TEST CONDITIONS	VALUES			UNIT
			min.	typ.	max.	
t_{THL}	transition time			400		ns
t_{TLH}	transition time			600		ns
$f_{\varnothing}$	clock frequency				500	KHz
C_I	input capacitance	$V_{OL} = V_{DD} = 0V$ f = 0.5...2 MHz			4	pF

• (over recommended operating conditions)

SCHEMATIC DIAGRAM



8 CHANNEL TOUCH CONTROL CIRCUIT FOR TV PROGRAM SELECTION

GENERAL DESCRIPTION

The MMP 710 circuit is used as input circuit together with the MMP 711 decoder circuit for electronic touch plate switching of 8 or 16 channels for TV program selection.
The MMP 710 circuit contains a 3 bit counter in p-channel high voltage technology. By any of the 8 inputs I_1 to I_8 it can be fixed in each state (parallel operation). The serial operation is accomplished on the H-L transitions of the clock pulse from the I_S input (clock impulses input). The binary coded output information is obtained from the push-pull output stages. When power-on, the counter is set on the 1 preferential state (HHH). In this basic operating mode the I_{CL} connection is tied to the V_{DD} potential and O4 to that of the background, V_{SS}. A 4 bit counter can be obtained by interconnecting 2 MMP 710 circuits. In this connection O4 has a combined input-output function. It controls by flip-flopping the operation of the 2 connected circuits. The disconnection of one of the 2 circuits is made by an internal connecting logic.
In this situation the I_{CL} connection of the first circuit is tied to the V_{DD} potential while that of the second circuit is tied to the background. The O1 ... O4 outputs and the I_S inputs of the 2 circuits are connected together.
All inputs are provided with integrated protective diodes.
The circuit is delivered in a 16 lead dual-in line plastic package..

FEATURES

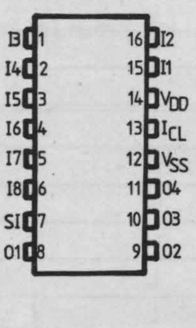
- Parallel and serial operation modes
- Preferencial output state at power-on
- Input protective diodes

ABSOLUTE MAXIMUM RATINGS

(T_A = 0 to 70°C)

V_{DD}	Supply voltage relative to V_{SS}	-31V to 0.3V
V_I	Input voltage relative to V_{SS}	-25V to 0.3V
T_A	Operating ambient temperature	0°C to 70°C
T_S	Storage temperature	-55°C to 125°C

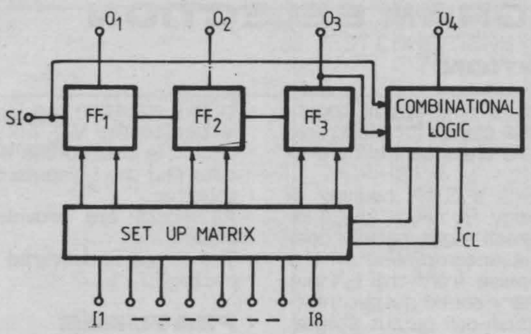
PIN CONNECTIONS



PIN NAMES

I1 I8	PARALLEL INPUTS
SI	SERIAL INPUT
O1 O4	OUTPUTS
ICL	INTERNAL CONNECTING LOGIC CONTROL
V_{DD}	POWER SUPPLY (-27^{-1}_{+2} V)
V_{SS}	GROUND

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

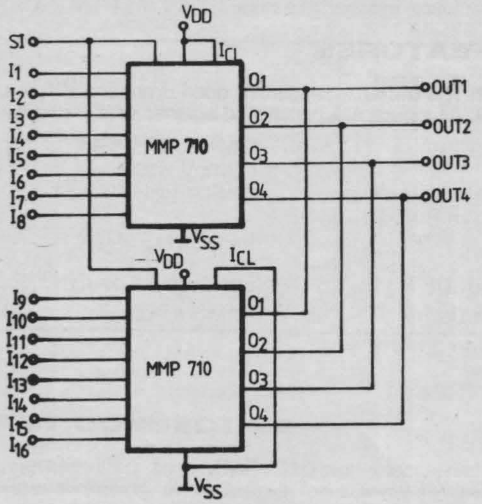
($-V_{DD} = 27^{+1}_{-2}$ V, $T_A = 25°C$)

PARAMETER	TEST CONDITION	VALUES min	VALUES max	UNIT
$-I_I$ Input leakage current	$-V_I = 25V$		10	μA
$-V_{IH}$ Input high voltage			2	V
$-V_{IL}$ Input low voltage		9		V
$-V_{OH}$ Output high voltage	$R_L = 100$ k		1	V
V_{OH}	$-I_O = 1$ mA		3	V
$-V_{OL}$ Output low voltage	$R_L = 100$ k	10		V
V_{OL}	$-I_O = 1$ mA	9		V
$-I_1$ Supply current	$I_O = 0$		2.3	mA

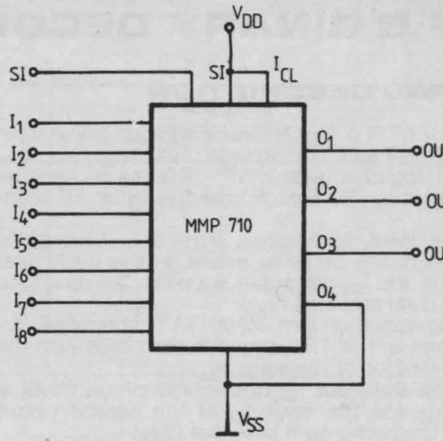
OUTPUT DATA

STATE	OUTPUT DATA O_1	O_2	O_3	O_4
1	H	H	H	H
2	L	H	H	H
3	H	L	H	H
4	L	L	H	H
5	H	H	L	H
6	L	H	L	H
7	H	L	L	H
8	L	L	L	H
9	H	H	H	L
10	L	H	H	L
11	H	L	H	L
12	L	L	H	I
13	H	H	L	L
14	L	H	L	L
15	H	L	L	L
16	L	L	L	L

TYPICAL APPLICATIONS

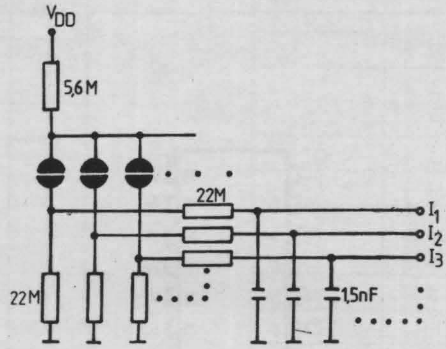


4 BITS COUNTER

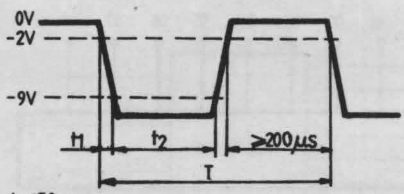


3 BITS COUNTER

INPUT CONNECTING TO TOUCH PLATES



CLOCK PULSE CHARACTERISTICS



$t_1 \leq 50 \mu s$
$t_2 = 60 \ldots 200 \mu s$
pause width $\geq 200 \mu s$

1 OF 8 BINARY DECODER

GENERAL DESCRIPTION

The MMP 711 is a 1 of 8 binary decoder manufactured in PMOS-Al gate high voltage technology.
MMP 711 together with MMP 710 can be used as output circuit for TV switch channels (8 or 16 channels).
The binary input information from the 4 inputs is transferred to the decoding matrix. In this basic operation mode the I_{CL} connexion is tied to V_{DD} and I_4 to the background potential (V_{SS}).
Assembling together two MMP 711 integrated circuits to form a 1 of 16 binary decoder needs with the proper connection of the input I_{CL}.
In this case the input I_{CL} of the first circuit (1...8) is tied to V_{DD} and the input I_{CL} of the second circuit (9...16) to the background potential (V_{SS}).
The inputs I_1...I_4 of both circuits are tied together.
The MMP 711 is supplied in a 16 lead dual in line plastic package.

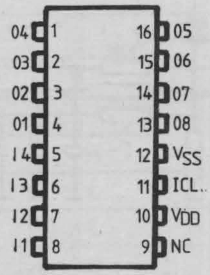
FEATURES

- The outputs consist of open drain transistors.
- All inputs are protected against static charge.

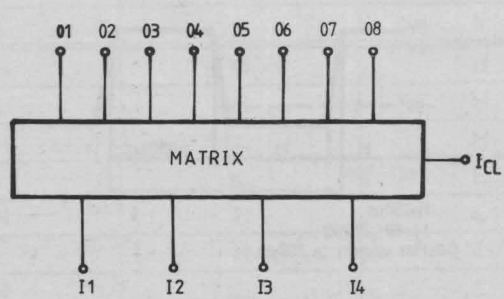
ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply Voltage	-31 ... +0.3	V
V_I	Input Voltage	-25 ... +0.3	V
I_O	DC Output Current	- 3	mA
T_A	Operating Ambient Temperature	0 ... +70	°C
T_{stg}	Storage Temperature	-55 ... +125	°C

PIN CONNECTIONS



BLOCK DIAGRAM



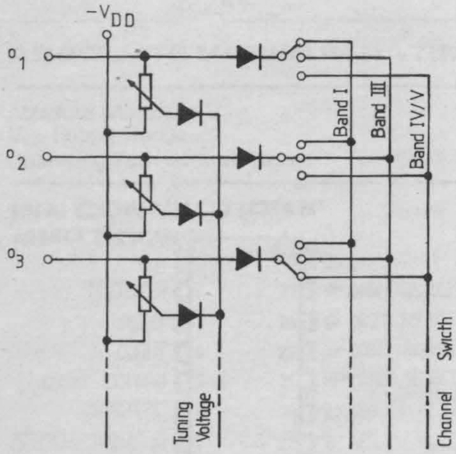
ELECTRICAL CHARACTERISTICS

($-V_{DD} = 27^{+1}_{-2}$ V, $T_A = 25°C$) unless otherwise specified

PARAMETER		TEST CONDITION	VALUES		UNIT
			min	max	
$-V_{IH}$	Input High Voltage			2	V
$-V_{IL}$	Input Low Voltage		9		V
$-V_{OH}$	Output High Voltage	$R_L = 100$ K		0.5	V
$-V_{OH}$		$-I_0 = 3$ mA		2	V
$-I_{DD}$	V_{DD} Supply Current	$I_0 = 0$		0.6	mA
$\frac{\Delta(V_{DD}-V_{OH})}{\Delta T_A}$	Output High Voltage Differential Drift	$T_A = 10...50°C$ $R_L = 100$ K		1	$\frac{mV}{°C}$

OUTPUT CONNECTING

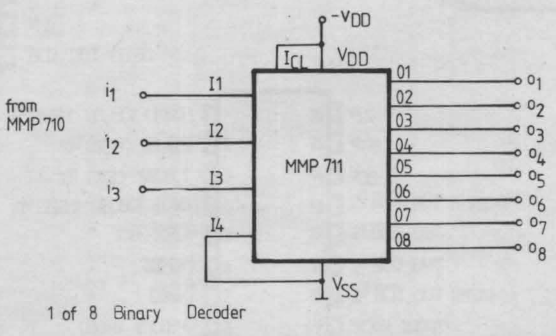
Used together with the MMP 710 for electronic touch plate switching of programs for television receivers.



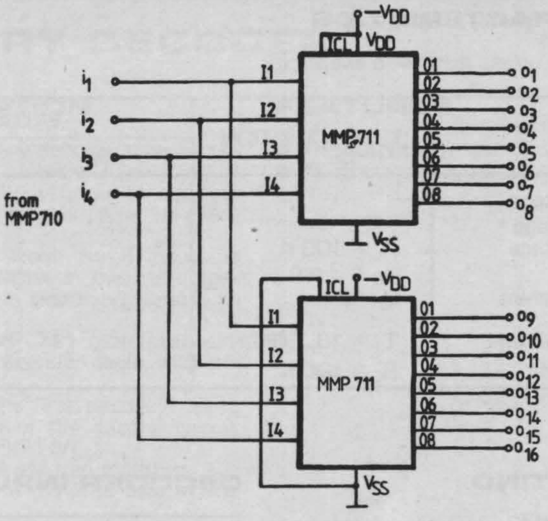
DECODER INPUT DATA

STATE	OUTPUT DATA			
	I_1	I_2	I_3	I_4
1	H	H	H	H
2	L	H	H	H
3	H	L	H	H
4	L	L	H	H
5	H	H	L	H
6	L	H	L	H
7	H	L	L	H
8	L	L	L	H
9	H	H	H	L
10	L	H	H	L
11	H	L	H	L
12	L	L	H	L
13	H	H	L	L
14	L	H	L	L
15	H	L	L	L
16	L	L	L	L

TYPICAL APPLICATIONS



1 of 8 Binary Decoder



1 of 16 Binary Decoder

4-DIGIT COUNTER / DISPLAY DECODER

GENERAL DESCRIPTION

The MMP 5002/5/7 is an ion-implanted, P-channel MOS, four-decade synchronous counter with latches, multiplexing circuits, and a read-only memory programmed for seven-segment outputs and BCD outputs. In addition many on-chip control circuits provide flexibility of use with a minimum of external components.
The MMP 5002/5/7 provides a means of counting up to 9999, transferring the count into latches without interrupting the counting operation, and supplying the latched information to the outputs one decade at a time Scanning is controlled by the SCAN input which increments a one-of-four counter on its negative edge, thereby scanning the latches from MSD (Most Significant Digit) to LSD (Least Significant Digit).
Low-threshold voltages for input DTL/TTL compatibility are achieved through the ion-implantation process. Enchancement mode devices as well as depletion-mode devices, are fabricated on the chip, allowing it to operate from a single +5 V power supply. Deppletion-mode technology also allows the entire circuit to operate on less than 25 mW of power The block diagram, shows all options available on the MMP 5002/5/7 Other members of this family which are different versions of this same chip are the MMP 5005 and MMP 5007. The MMP 5005 is supplied in a 24-pin pakage and does not include the BCD outputs. The MMP 5007 is supplied in a 16-pin package.

FEATURES

- Single-supply operation or double-supply for higher output drive
- Multiplexed seven-segment and/or BCD outputs
- TTL-compatible inputs
- Four decades of synchronous counting
- Minimum external component count
- Low power consumption

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum V_{SS}	7,5 V
V_{GG} Supply Range	0V V_{GG} −13,2 V
Operating Temperature Range	0°C T_A 75°C

PIN CONNECTIONS

MMP 5002

1	V_{GG}	28	V_{SS}
2	$\overline{\text{TRANSFER}}$	27	10^0 DIGIT SELECT OUTPUT (LSD)
3	RESET	26	10^1 DIGIT SELECT OUTPUT
4	$\overline{\text{COUNT}}$	25	10^2 DIGIT SELECT OUTPUT
5	COUNT EXTEND	24	10^3 DIGIT SELECT OUTPUT (MSD)
6	$\overline{\text{OVERFLOW}}$	23	"A" SEG (7-SEGMENT OUTPUTS)
7	$\overline{\text{DECIMAL POINT IN}}$	22	"B" SEG (7-SEGMENT OUTPUTS)
8	DECIMAL POINT LEFT OR RIGHT	21	"C" SEG (7-SEGMENT OUTPUTS)
9	$\overline{\text{BLANKING}}$	20	"D" SEG (7-SEGMENT OUTPUTS)
10	SCAN INPUT	19	"E" SEG (7-SEGMENT OUTPUTS)
11	TRUE/COMPLEMENT	18	"F" SEG (7-SEGMENT OUTPUTS)
12	$\overline{\text{BCD}}$ OUT (MSB)	17	"G" SEG (7-SEGMENT OUTPUTS)
13	$\overline{\text{BCD}}$ OUT 2^2	16	V_{DD}
14	$\overline{\text{BCD}}$ OUT 2^1	15	BCD OUT (LSB)

MMP 5005

1	V_{GG}	24	V_{SS}
2	$\overline{\text{TRANSFER}}$	23	10 DIGIT SELECT OUTPUT (LSD)
3	$\overline{\text{RESET}}$	22	10 DIGIT SELECT OUTPUT
4	$\overline{\text{COUNT}}$	21	10 DIGIT SELECT OUTPUT
5	COUNT EXTEND	20	10 DIGIT SELECT OUTPUT (MSD)
6	$\overline{\text{OVERFLOW}}$	19	A SEG (7-SEGMENT OUTPUTS)
7	$\overline{\text{DECIMAL POINT IN}}$	18	B SEG (7-SEGMENT OUTPUTS)
8	DECIMAL POINT LEFT OR RIGHT	17	C SEG (7-SEGMENT OUTPUTS)
9	$\overline{\text{BLANKING}}$	16	D SEG (7-SEGMENT OUTPUTS)
10	SCAN INPUT	15	E SEG (7-SEGMENT OUTPUTS)
11	TRUE/COMPLEMENT	14	F SEG (7-SEGMENT OUTPUTS)
12	V_{DD}	13	G SEG (7-SEGMENT OUTPUTS)

MMP 5007

1	10^3 DIGIT SELECT (MSD)	16	V_{SS}
2	10^2 DIGIT SELECT	15	V_{GG}
3	10^1 DIGIT SELECT	14	V_{DD}
4	10^0 DIGIT SELECT (LSD)	13	2^0 $\overline{\text{BCD}}$ OUT (LSB)
5	$\overline{\text{TRANSFER}}$	12	2^1 $\overline{\text{BCD}}$ OUT
6	$\overline{\text{RESET}}$	11	2^2 $\overline{\text{BCD}}$ OUT
7	$\overline{\text{COUNT}}$	10	2^3 $\overline{\text{BCD}}$ OUT (MSB)
8	COUNT EXTEND	9	SCAN INPUT

RECOMANDED OPERATING CONDITIONS

PARAMETER	TEST CONDITIONS	VALUES min.	VALUES typ.	VALUES max.	UNITS	NOTES
V_{SS} Supply voltage	V_{SS}—V_{DD}	4.5	5.0	7.5	V	1.2
V_{GG} Supply voltage	V_{GG}—V_{DD}	−13.2	−12	V_{DD}	V	1.2
F_{CI} Count frequency		dc		250	kHz	

STATIC ELECTRICAL CHARACTERISTICS

($V_{SS} = +5$ V ±5%; $V_{GG} = V_{DD} = 0$ V; 0°C≤T_A≤70°C unless otherwise noted)

PARAMETER	VALUES min.	VALUES typ.	VALUES max.	UNITS	NOTES
V_{IL} Input voltage, logic "0" (Low)		V_{DD}	V_{DD}+0.8	V	
V_{IH} Input voltage, logic "1" (High)	V_{SS}−1	V_{SS}	V_{SS}+0.3	V	3
I_{SS} Supply current, V_{SS}		2.5	5.0	mA	4, Inputs open
I_{GG} Supply current, V_{GG}		0.2	0.5	mA	$V_{GG} = -12$ V
C_{IN} Input capacitance		3	10	pF	$T_A = 25$°C; f = 1 MHz, $V_{IN} = V_{SS}$
I_{IL} Input current, logic "0" Count input			1.6	mA	5
Scan input			1.6	mA	5
Decimal point input			1.0	μA	
Other logic inputs			1.0	mA	
I_{OL} Output current, logic "0"	0.5			mA	6, $V_{GG} = -12$ V
I_{OH} Output current, logic "1"	0.5			mA	6, $V_{GG} = -12$ V
V_{OL} Output voltage, logic "0"			V_{DD}+0.2	V	4
V_{OH} Output voltage, logic "1"	V_{SS}—0.2			V	4

DYNAMIC ELECTRICAL CHARACTERISTICS

($V_{SS} = +5$V ±5%; $V_{GG} = V_{DD} = 0$ V; 0°C≤T_A≤70°C unless otherwise noted)

PARAMETER	VALUES min.	VALUES typ.	VALUES max.	UNITS	NOTES
f_{CI}—Count input frequency	dc		250	kHz	
f_{SI}—Scan input frequency	dc		50	kHz	
t_{RD} Reset to any output delay			15	μs	
t_{PW} Logic "0", Pulse width, Reset input	1.0			μs	
Count input	1.0				
Scan input	10.0				
Transfer input	2.5				
t_{PH} Logic "1" time, Count input	3.0			μs	
Scan input	10.0				
t_{SD} Scan to output disable time Digit select outputs			15	μs	7
All data outputs			15		7
t_{SE} Scan to output enable time Digit select outputs			15	μs	8
All data outputs			15		8

PARAMETER	VALUES			UNITS	NOTES
	min.	typ.	max.		
t_{CE} Count input to count extend delay to 1 or 0			15	μs	9
t_{OF} Count input to overflow delay (ON)			15	μs	9
t_{ROF} Reset input to overflow delay (OFF)			5	μs	

NOTES

1. $V_{DD} = 0$ V
2. V_{SS}—V_{GG} no more than 20.7 V
3. Internal pull-up resistors (aprox. 10 K) are provided at all inputs other than Count input, Scan input, and Decimal point input
4. $V_{GG} = -12$ V ±10%. Outputs open
5. Measurement made at $V_I = V_{DD} + 0.4$ V. This condition is sufficient to represent a logic 0 and hold off or override the internal oscillators. Maximum current at $V_I = +0.4$ V is 1.6 mA. 400 μA source current at V_{SS}—1.0 V is sufficient to represent a logic "1" and hold off or override the internal oscillators.
6. I_{OL} measured at $V_O = V_{SS} - 0.75$ V (Direct driving base pnp emitter to V_{SS})
   I_{OH} measured at $V_O = V_{DD} + 0.75$ V (Direct driving base npn emitter to V_{DD})
7. Delay measured from the negative edge of the SCAN input.
8. Delay measured from the rising edge of the SCAN input.
9. Delay measured from the negative edge of the COUNT input.

FUNCTIONAL DESCRIPTION

V_{GG}, Pin 1

V_{GG} is the output gate drive voltage supply which is no greater than V_{DD} and no less than V_{DD}—13.2 V. Higher output drive capability is realized when V_{GG} is maintained at the recommended level of V_{DD}−12 V.

$\overline{\text{TRANSFER}}$, Pin 2

While $\overline{\text{TRANSFER}}$ is at logic 0, data in the decade counters is continuously transferred to the latches. This input may be left at 0 for a continuous transfer and display mode or may be driven high to subsequently cause the latches to store the current counter contents. Storage occurs internally when $\overline{\text{TRANSFER}}$ is taken to a 1 and the next negative edge of $\overline{\text{COUNT INPUT}}$ occurs. This allows asynchronous $\overline{\text{COUNT}}$ and $\overline{\text{TRANSFER}}$ operation since the transfer is terminated internally prior to incrementing the counters. This means that a $\overline{\text{COUNT}}$ negative edge must follow a $\overline{\text{TRANSFER}}$ command before a reset is applied to assure transfer of valid data. An external reset command must be delayed at least one $\overline{\text{COUNT}}$ negative edge following a transfer. External transfer should terminate at least 1 μs prior to this $\overline{\text{COUNT}}$ negative edge and $\overline{\text{RESET}}$ should occur no sooner than 1 μs following that edge.

$\overline{\text{RESET}}$, Pin 3

The decade counters are reset to 0000 when $\overline{\text{RESET}}$ is at logic 0. The $\overline{\text{RESET}}$ input at logic 0 also forces the scan counter to the MSD output and resets the $\overline{\text{OVERFLOW}}$ latch output to a logic 1. It maintains this condition as long as a logic 0 is present at $\overline{\text{RESET}}$ and overrides all other associated inputs. As indicated previously, the decade counters should not be reset until a transfer has been terminated.

Since the $\overline{\text{RESET}}$ input resets the scan counter to the MSD, the scan rate must be much faster than the reset rate to allow the lesser significant digits to be enabled. Therefore, F_{SCAN} should be much greater than four times f_{RESET}.

Ideally, the reset pulse should also be made narrow to prevent its duration from causing the MSD to be on much longer than the other digits and thus appear to be brighter.

$\overline{\text{COUNT}}$, Pin 4

The decade counters are synchronously incremented on the negative edge of the $\overline{\text{COUNT}}$ input. The internal oscillator on this input may be overridden by an external signal source or may be allowed to oscillate at a frequency set by a single capacitor tied to this input from the V_{SS} or V_{DD} supply. In systems with considerable noise, better oscillator stability exists when the capacitor is tied to V_{SS}.

COUNT EXTEND, pin 5

COUNT EXTEND is a feature provided to enable MMP 5002s to be cascaded. Whenever the counter state attains 9999 count, the COUNT EXTEND output goes high. This output remains logical 1 only the next negative transition of $\overline{\text{COUNT}}$ OCCURS or a $\overline{\text{RESET}}$ signal is applied.

$\overline{\text{OVERFLOW}}$,Pin 6

$\overline{\text{OVERFLOW}}$ occurs on the 10,000th count input following a reset. It is normally high and, when activated, goes low to indicate that the decade counters have gone from 9999 to 0000 without encountering a reset. Once activated, the $\overline{\text{OVERFLOW}}$ latch will remain low until $\overline{\text{RESET}}$ is pulled low.

$\overline{\text{DECIMAL POINT}}$ IN, Pin 7

With $\overline{\text{DECIMAL POINT}}$ IN held high, the device employes leading zero blanking. This causes any leading zeros in the display latches to be blanked when their DIGIT SELECT goes high. At the start of each MSD to LSD scan, blanking of leading zeros occurs until the first non-zero number occurs in the display or $\overline{\text{DECIMAL POINT}}$ IN is clocked to a 0. Any number following will be displayed. Leading zero blanking does not affect the $\overline{\text{BCD}}$ outputs or the LSD in the Display which is displayed even if zero.
Tehe LSD output resets the blanking circuitry to begin blanking zeros in the next scan cycle.
Leading zero blanking may be inhibited by wiring $\overline{\text{DECIMAL POINT}}$ IN to ground. The MMP 5007 does not have a pin for $\overline{\text{DECIMAL POINT}}$ IN and therefore does not have leading zero blanking.
In the DECIMAL POINT RIGHT mode, even though the $\overline{\text{DECIMAL POINT}}$ IN is clocked, unblanking is delayed until the following digit is enabled.

DECIMAL POINT LEFT OR RIGHT,Pin 8

Bringing this control to logic 1 allows the use of displays with the decimal point physically located on the left side of the numeral.
Logic 0 on this input allows for a right-handed decimal point.

$\overline{\text{BLANKING}}$, Pin 9

The $\overline{\text{BLANKING}}$ input at logic 0 forces the 7-segment outputs to the off-state and the $\overline{\text{BCD}}$ to the equivalent of the number zero. This condition is maintained on a dc basis as long as the $\overline{\text{BLANKING}}$ input is zero. The DIGIT SELECT outputs continue to operate at the scan rate as described.

SCAN INPUT, Pin 10

The DIGIT SELECT COUNTER is incremented by a negative edge on the SCAN INPUT. During the time the SCAN INPUT is at 0, the SEGMENT and DIGIT SELECT outputs are forced off and the complement $\overline{\text{BCD}}$ outputs are forced to logic 1. The off level of the 7-segment and $\overline{\text{BCD}}$ outputs is determined by the state of the TRUE/COMPLEMENT input. This remains until the SCAN INPUT returns to logic 1.
The DIGIT SELECT COUNTER is a one-of-four counter, scanning from MSD to LSD, enabling one quad latch output at a time, and presenting a logic 1 to the corresponding DIGIT SELECT output.
The internal oscillator on this input may be overridden by an external signal source or may be allowed to oscillate at a frequency set by a single capacitor tied to this input from the V_{SS} or V_{DD} supply. In systems with considerable noise better oscillator stability exists when the capacitor is tied to V_{SS}.

TRUE/COMPLEMENT, Pin 11

When this control is driven to 0, inversion of both the $\overline{\text{BCD}}$ and 7-segment outputs occurs. Depending upon the display used, combinations of the $\overline{\text{BLANKING}}$ input and TRUE/COMPLEMENT control can be chosen to give a lamp test.

$\overline{\text{BCD}}$ OUT, Pins 12 through 15

The $\overline{\text{BCD}}$ outputs are push-pull and are designed to drive directly to the base of common emitter transistors.

V_{DD}, Pin 16

V_{DD} is the negative supply and is nomimally ground.

SEGMENT OUTPUTS, Pins 17 through 23

The SEGMENT OUTPUT buffers are identical to the $\overline{\text{BCD}}$ output buffers.

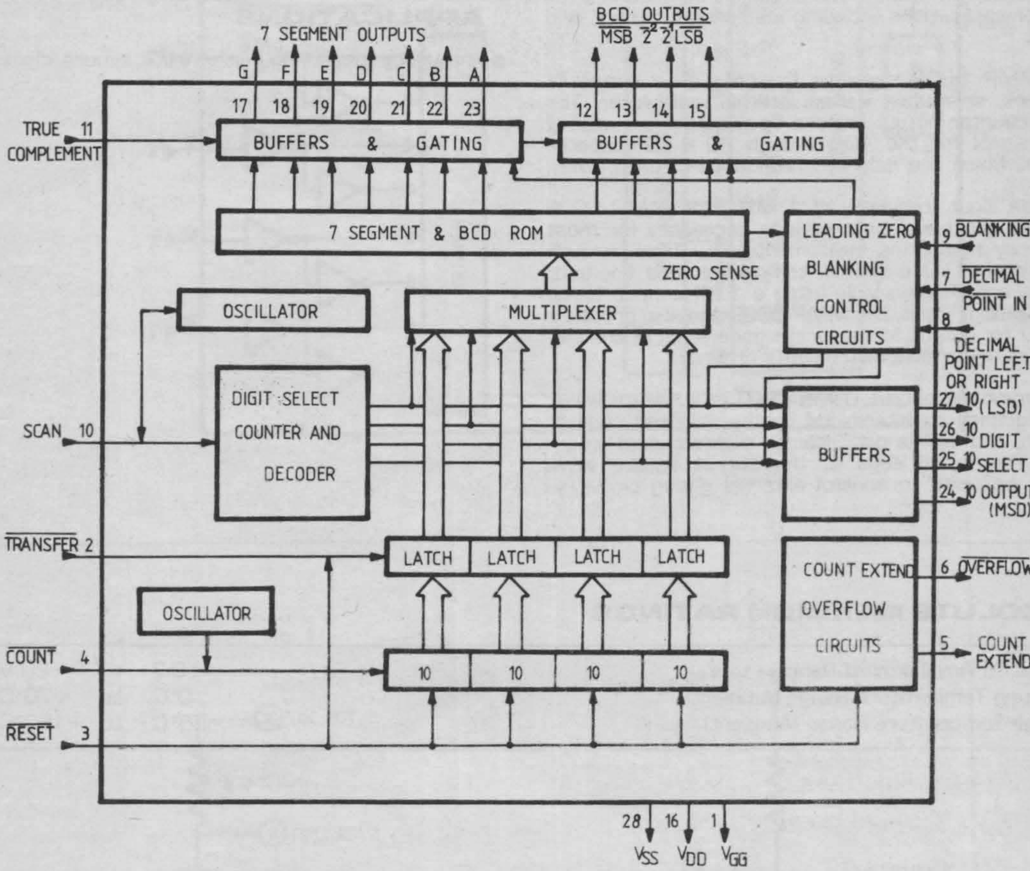
DIGIT SELECT OUTPUTS, Pins 24 through 27

The DIGIT SELECT OUTPUTS are push-pull and go high during their appropriate times to accomplish the multiplexing of the digits.

V_{SS}, Pin 28

V_{SS} is the positive supply voltage and is nominally maintained at 5 Vdc with respect to V_{DD}.

BLOCK DIAGRAM



COUNTER TIME - BASE CIRCUIT

GENERAL DESCRIPTION

The MMP 5009 is a highly versatile MOS oscillator and divider chain manufactured in the depletion-load ion implantation process and P-channel technology. The 16-pin DIP package provides frequency division ranges from 1 to 36 x 10^8. The circuit will operate from any of three frequency sources: the internal oscillator with an external RC combination; the internal oscillator with an external crytal; or with an externally-applied TTL signal. Control inputs provide additional versatility and allow the circuit to be used in a variety of applications including instrumets, timers and clocks.

The MMP 5009 consists basically of a series of counters, selectable via an internal multiplexer. The $\div 10^1$ counter output is used to generate an internal clock signal for the 10^2 through 36 x 10^8 counter stages, which are fully synchronous with each other.

With an input frequency of 1 MHz, the MMP 5009 provides the basic time periods necessary for most frequency measuring instruments, i.e., 1 µs through 100 seconds. One-minute, ten-minute, and one-hour periods are also available using a 1 MHz input. Using a 1/1.2 MHz input, the MMP 5009 can also provide a 50/60 Hz output for accurate generation of line frequencies in portable instruments or clocks.

The time-base output (TIME OUT) is a square wave; its frequency is determined by the selected counter division, and by the oscillator or external input frequency. The falling edge of the output square wave should be used to control external gating circuitry..

FEATURES

- Ion-implanted for full TTL/DTL compatibility
- Internal clock operates from:
  External signal
  External RC network
  External crystal
- Operates dc to above 1 MHz
- Binary-encoded for frequency selection
- Resettable to highest or lowest state
- Twenty different modes of division

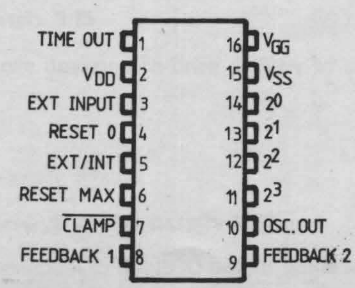
APPLICATIONS

- Frequency measuring instruments, timers, clocks.

ABSOLUTE MAXIMUM RATINGS

Voltage On Any Terminal Relative to V_{SS}	+0.3	to	−20 V
Operating Temperature Range (Ambient)	0°C	to	+70°C
Storage Temperature Range (Ambient)	−55°C	to	+150°C

PIN CONNECTIONS



BLOCK DIAGRAM

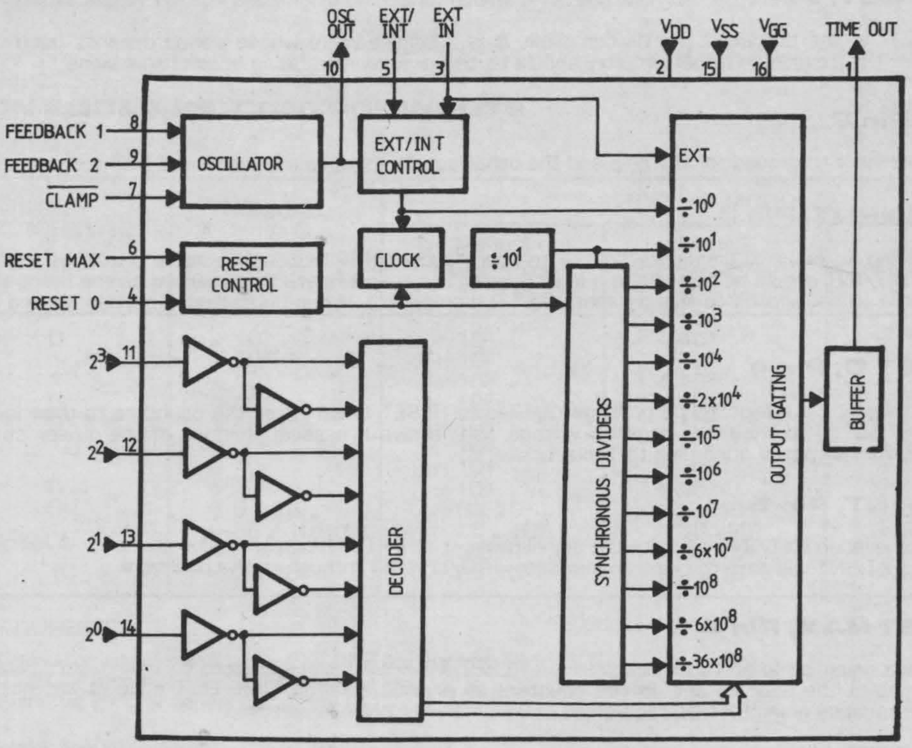


Fig. 1

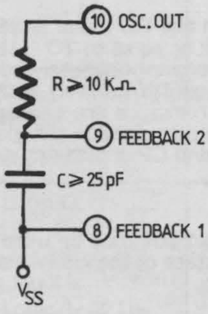
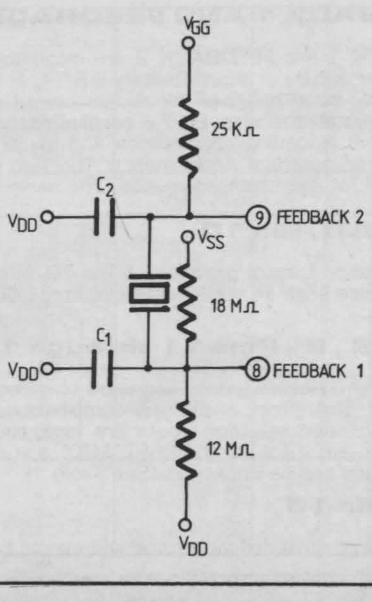


Fig. 2



FUNCTIONAL DESCRIPTION

TIME OUT, Pin 1

TIME OUT is the output of the divider chain. It is a square wave whose period depends upon the division mode. For this reason, external circuitry should be triggered on the falling edge of this signal.

V_{DD}, Pin 2

V_{DD} is normally to ground for the chip and the other supply voltages are measured with respect to V_{DD}.

EXT INPUT, Pin 3

When using an external frequency source to operate the MMP 5009, that signal should be applied at EXT IN and EXT/INT should be brought to a logic 1 level. The counters are incremented on the falling edge of EXT IN and the signal applied to this pin must be TTL-compatible. When unused, this pin can be tied either high or low.

RESET O, Pin 4

A positive-going pulse of 10 µs or longer applied to RESET O will reset the counters to their lowest state. Taking RESET O to the most negative voltage, V_{GG}, allows bypassing portions of the divider chain for testing or other purposes according to Table 1.

EXT/INT, Pin 5

A logic 1 level on EXT/INT will gate the signal present at EXT/INthrough to the counters. A logic O level applied to EXT/INT will gate the internal oscillator (RC/crystal) through to the counters.

RESET MAX, Pin 6

A positive going pulse of 10 µs or longer on RESET MAX will reset counters to their highest state. RESET MAX enables the user to set up the counters to provide a falling TIME OUT edge at the next oscillator cycle or negative going EXT IN, regardless of which divider chain is selected.

Taking RESET MAX to the most negative voltage, V_{GG}, allows bypassing portions of the divider chain for testing or for other purposes given in Table 1.

$\overline{\text{CLAMP}}$, Pin 7

$\overline{\text{CLAMP}}$ is used in conjunction with the RC mode of operation. Its purpose is to provide accurate start-up operations.

When $\overline{\text{CLAMP}}$ is taken to a logic O level, the internal circuitry is held at a fixed reference voltage. Then, when $\overline{\text{CLAMP}}$ is taken to a logic 1 level the oscillator's first cycle will be a full cycle.

FEEDBACK 1 AND FEEDBACK 2, Pins 8 and 9

FEEDBACK 1 and FEEDBACK 2 are oscillator ports. Operation in the RC mode is acieved as shown in Figure 1 Frequency is approximately 0.8/RC.R must be greater than or equal to 10 kΩ and C must be greater than or equal to 25 pF for proper operation. Operation in the crystal oscillator mode is shown in Figure 2. The crystal operates in the parallel resonant mode, should operate properly with a 5 mW drive, and should have a loading capacitance (C_L) of 32 pF. Values for the resistors are chosen to bias the internal circuitry for optimum performance. The two capacitors are chosen to provide the loading capacitance (C_L) specified for the selected crystal. The series combination of C1 and C2 should not exceed the value of C_L.

OSC OUT, Pin 10

The oscillator output, provided at Pin 10, is not a true logic output but may be used to drive a high impedance device such as other MOS circuitry OSC OUT reflects the state of the internal oscillator.

2^3, 2^2, 2^1, 2^0, Pins 11 through 14

The division selector inputs are used to select the ratio of the TIME OUT frequency to the oscillator input frequency. The effect of specific combinations of logic levels on these pins is shown in Table 1. Note that when all division selector inputs are high, the signal applied to EXT IN appears at the TIME OUT output. Also when RESET O and RESET MAX are used in conjunction with the division selector inputs, several more modes can be accessed. (See Table 1)

V_{SS}, Pin 15

V_{SS} is the positive supply voltage and should be maintained at 5 Vdc ±10% with respect to V_{DD}.

V_{GG}, Pin 16

V_{GG} is the negative supply voltage and should be maintained at −12 Vdc with respect to V_{DD}.

DIVISION MODES VS. CONTROL INPUTS

Table 1

DIVISION SELECTORS*				NORMAL Mode 0 $R_{MAX} = 0$ $R_0 = 0$	BYPASS MODES		
2^3	2^2	2^1	2^0		Mode 1 $R_{MAX} = V_{GG}$ $R_0 = 0$	Mode 2 $R_{MAX} = 0$ $R_0 = V_{GG}$	Mode 3 $R_{MAX} = V_{GG}$ $R_0 = V_{GG}$
0	0	0	1	$\div 10^1$	$\div 10^1$	$\div 10^1$	$\div 10^1$
0	0	1	0	$\div 10^2$	$\div 10^2$	$\div 10^2$	$\div 10^2$
0	0	1	1	$\div 10^3$	$\div 10^3$	$\div 10^3$	$\div 10^3$
0	1	0	0	$\div 10^4$	$\div 10^4$	$\div 10^4$	$\div 10^4$
0	1	0	1	$\div 10^5$	$\div 10^2$	$\div 10^5$	$\div 10^2$
0	1	1	0	$\div 10^6$	$\div 10^3$	$\div 10^6$	$\div 10^3$
0	1	1	1	$\div 10^7$	$\div 10^4$	$\div 10^7$	$\div 10^4$
1	0	0	0	$\div 10^8$	$\div 10^5$	$\div 10^5$	$\div 10^2$
1	0	0	1	$\div 6 \times 10^7$	$\div 6 \times 10^4$	$\div 6 \times 10^4$	$\div 6 \times 10^1$
1	0	1	0	$\div 36 \times 10^8$	$\div 36 \times 10^5$	$\div 36 \times 10^5$	$\div 36 \times 10^2$
1	0	1	1	$\div 6 \times 10^8$	$\div 6 \times 10^5$	$\div 6 \times 10^5$	$\div 6 \times 10^2$
1	1	1	0	$\div 2 \times 10^4$	$\div 2 \times 10^1$	$\div 2 \times 10^1$	$\div 2 \times 10^1$

* SPECIAL ADDRESSES

0000 — Oscillator signal selected by EXT/INT appears at TIME OUT
1100 or 1101 — Forces TIME OUT to logic 0 level
1111 — Signal at EXT IN appears at TIME OUT

Logic 1 = High = V_{SS}
Logic 0 = Low = V_{DD}

DC ELECTRICAL CHARACTERISTICS

($V_{SS} = +5$ V ± 10%; $V_{DD} = 0$ V; $V_{GG} = -12.0$ V ± 20%; 0°C ≤ T_A ≤ 70° C)

	PARAMETER	VALUES min.	typ.●	max.	UNITS	NOTES
V_{SS}	Supply Voltage	+4,5		+5,5	V	
V_{DD}	Supply Voltage	0,0		0,0	V	
V_{GG}	Supply Voltage	−14,4		−9.6	V	
I_{SS}	Supply Current, V_{SS}		6,0	11.0	mA	Note 1
I_{GG}	Supply Current, V_{GG}		6,0	11.0	mA	
R	Feedback Resistance	0,01		2,5	M	
V_{IL}	Input Voltage, Logic 0,					
	Reset Inputs	0,0		0,8	V	
	Reset (Bypass Mode)	V_{GG}		$V_{GG}+1,0$	V	Note 2
	All Other Logic Inputs			0,8	V	
V_{IH}	Input Voltage, Logic 1, All Logic Inputs	V_{SS}–1.0	V_{SS}	V_{SS}+0,3	V	
I_{IL}	Input Current, Logic 0			−1,6	mA	Note 2 VI =0,4 V
V_{OL}	Output Voltage, Logic 0			0,4	V	I_{OL} = 1,6 mA
V_{OH}	Output Voltage, Logic 1	2,4			V	I_{OH} = 40 μA*

AC CHARACTERISTICS

($V_{SS} = +5\ V \pm 10\%$; $V_{DD} = 0V$; $V_{GG} = -12.0V \pm 20\%$; $0°C \leq T_A \leq 70°\ C$)

PARAMETER		VALUES			UNITS	NOTES
		min.	typ.●	max.		
f_{XTAL}	Crystal Frequency	0,1		2,0	MHz	
f_{RC}	RC Frequency	dc		200	kHz	
f_{EXT}	External Frequency	dc		2,0	MHz	
t_{PL}	Logic 0 Pulse Width, $\overline{CLAMP}$	1/2fOSC				Note 5
	EXT INPUT	200			ns	
t_{PH}	Logic 1 Pulse Width. EXT INPUT	200			ns	
	RESET MAX	10.0			µs	
	RESET 0	10.0			µs	
f_{STA}	Frequency Stability					
	w/Volt Change, RC Mode		±3.0		%/V	Note 3
	w/Temp. Change, RC Mode		−0.2		%/°C	Note 4
	Crystal Mode		—			
t_{ee}	Jitter, Edge-to-Edge Variation		<15		ns	Temp. & Supply Voltage Constant

NOTES

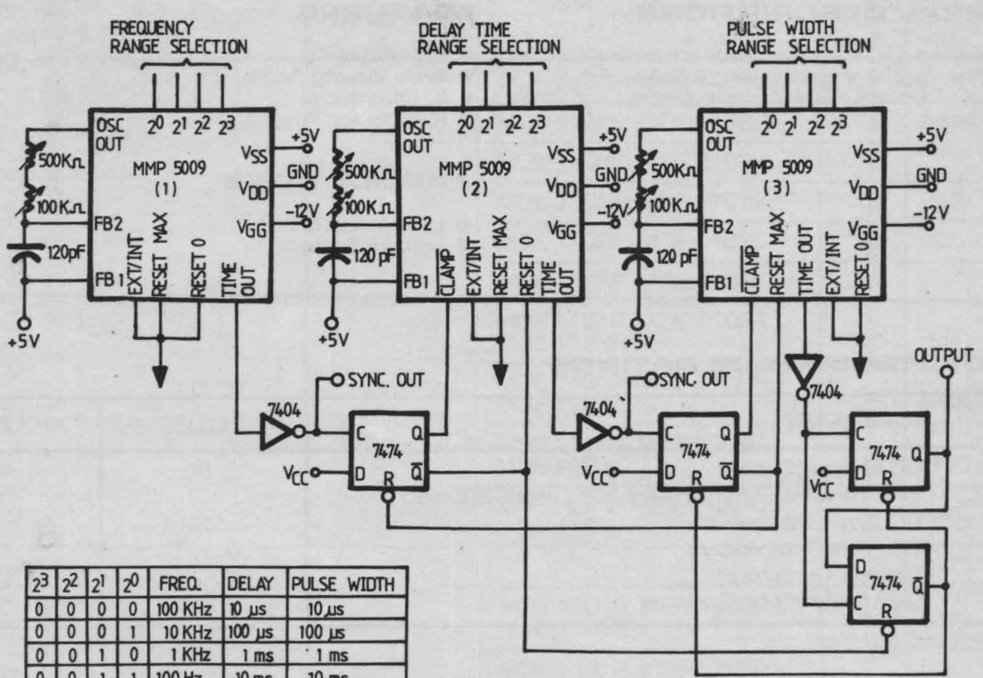
● Typical values at $V_{SS} = +5V$, $V_{DD} = 0V$, $V_{GG} = -12\ V$, and $T_A = 25°C$.
1. Logic inputs at V_{SS}, output open-circuited. Each logic input (See Note 2) contributes an additional 1.6 mA (max) to I_{SS} when at logic 0 level.
2. Logic inputs are: $\overline{RESET}$ MAX; $\overline{RESET}$ 0; Address inputs; EXT INPUT ; EXT/INT; and $\overline{CLAMP}$.
3. Frequency variations due to power supply changes only.
4. Crystal mode stability is dependent upon crystal.
5. Minimum logic 0 time at $\overline{CLAMP}$ input is 50% of oscillator period. (f_{OSC} = oscillator frequency)

* V_{OH}, V_{OL} apply only to TIME OUT.

PULSE GENERATOR

An extremely versatile pulse generator requiring few components is easily built using the MMP 5009. Three MMP 5009 circuits are used, as shown in Figure 3 . to provide the three essential pulse generator elements: (1) a frequency source to determine pulse repetition rate; (2) a variable time delay; and (3) a pulse width generation.
This circuit provides repetition rates from 0.1 Hz to 100 KHz with delay times and pulse widths from 10 µs to 10 seconds. Range selection is obtained by selecting the appropiate dividers, so that only three RC circuits are required. This eliminates the requirement for a different RC combination for each decade, commonly found in commercial instruments. Decade selection is accomplished by a binary code at the inputs to each MMP 5009 which could be provided by a coded rotary or thumbwheel switch. The vernier control is a 500K potentiometer. A 100K potentiometer is used as a trimmer for initial calibration. External TTL control logic is used to capture the accurately controlled negative edges as they emerge from each MMP 5009. The Reset and $\overline{Clamp}$ Inputs allow synchronization and first-cycle accuracy from the time-base circuits.
Other features can be added to the basic circuitry shown in Figure 2. For example, the output amplitude can be made adjustable by using high voltage, open-collector TTL circuitry with potentiometer control for amplitude. An extra position can be used on the frequency selection switch for an external trigger source. This trigger source should be connected to the first control D-type latch instied of the output from the 5009 (1) The frequency range may even be extended to 1.0 MHz with time delays reduced to 1µs, although some loss in RC stability would occur since the recommended data sheet frequency has been exceeded.

Fig. 3



2^3	2^2	2^1	2^0	FREQ.	DELAY	PULSE WIDTH
0	0	0	0	100 KHz	10 µs	10 µs
0	0	0	1	10 KHz	100 µs	100 µs
0	0	1	0	1 KHz	1 ms	1 ms
0	0	1	1	100 Hz	10 ms	10 ms
0	1	0	0	10 Hz	100 ms	100 ms
0	1	0	1	1 Hz	1 s	1 s
0	1	1	0	0.1 Hz	10 s	10 s

STANDARD LIGHT EMITTING DIODES

GENERAL DESCRIPTIONS

The Standard LED s (Ø = 5 mm) are visible sources (red, amber, yellow or green) using a $GaAs_{1-x}P_x$ (x = 0, .1) They are made in planar process and epoxy encapsulated.

FEATURES

- High Intensity
- Wide Viewing Angle
- IC Compatible
- Reliable and Rugged.

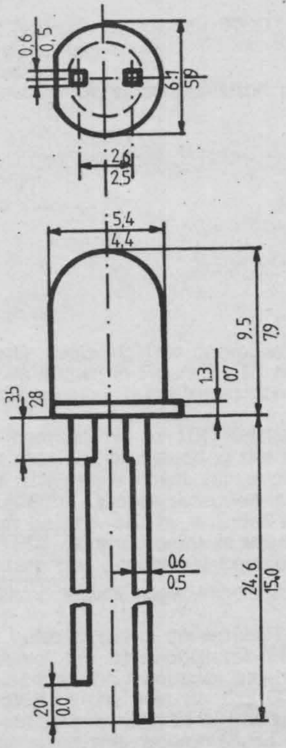
APPLICATIONS

- Light Indicators
- Voltage Sensors

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	VALUES	UNIT
I_{Fmax}	DC Forward Current	50	mA
$I_{Fpeak\ max}$	Peak Forward Current (1 μsec pulse width, 300 pps)	1	A
P_{dmax}	DC Power Dissipation	150	mW
T_A	Operating Temperature	0...+70	°C
T_{stg}	Storage Temperature	−40...+85	°C
T_{ead}	Lead Soldering Temperature	+260	°C

PACKAGE DIMENSIONS

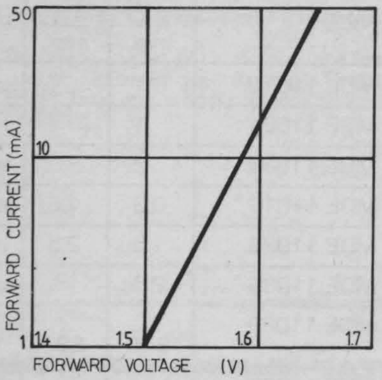


OPTOELECTRIC CHARACTERISTICS AT $T_A = 25°C$

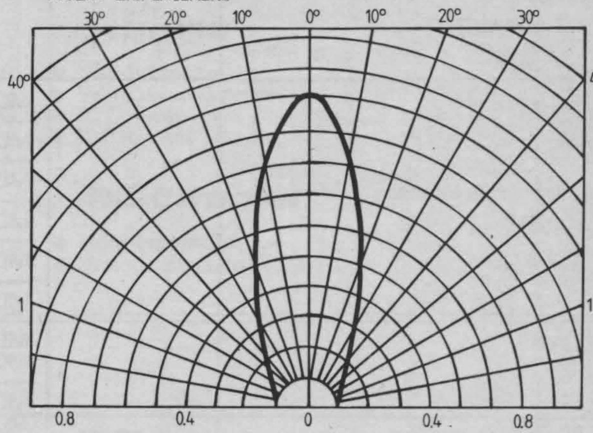
PARAMETER	TEST CONDITIONS	DEVICE	VALUES min.	VALUES max.	UNIT
I_V Luminous Intensity	$I_F = 20$ mA	MDE 1101R, MDE 1101V	0,1	1	mcd
		MDE 1102R, MDE 1102V	1	2	mcd
		MDE 1103R, MDE 1103V	2		mcd
		MDE 1101P, MDE 1101G	0,3	1,5	mcd
		MDE 1102P, MDE 1102G	1,5	2,5	mcd
		MDE 1103P, MDE 1103G	2,5		mcd
λ_p Peak Wavelength	$I_F = 20$ mA	MDE 1101R, MDE 1102R, MDE 1103R	645	680	nm
		MDE 1101P, MDE 1102P, MDE 1103P	625	640	nm
		MDE 1101G, MDE 1102G, MDE 1103G	573	590	nm
		MDE1101V, MDE 1102V, MDE 1103V	554	570	nm
$\theta_{1/2}$ Viewing Angle	$I_F = 20$ mA		40		grad
V_F Forward Voltage	$I_F = 20$ mA	MDE 1101R, MDE 1102R, MDE 1103R		2	V
		MDE 1101P, MDE 1102P, MDE 1103P MDE 1101G, MDE 1102G, MDE 1103G MDE1101V, MDE 1102V, MDE 1103V		3	V
BV_R Reverse Breakdown Voltage	$I_R = 100\ \mu A$		3		V
C_o Capacitance	$V_F = 0$ V f = 1 MHz	MDE 1101R, MDE 1102R, MDE 1103R		70	V
		MDE 1101P, MDE 1102P, MDE 1103P MDE 1101G, MDE 1102G, MDE 1103G MDE1101V, MDE 1102V, MDE 1103V		60	pF

Note: R — red
V — green
G — yellow
P — amber

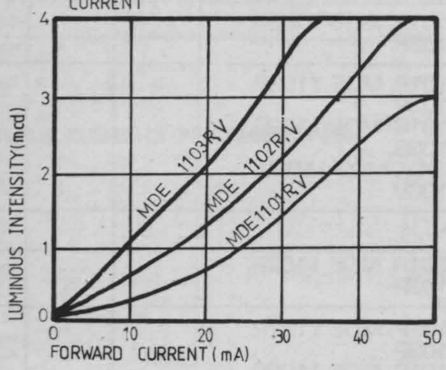
FORWARD CURRENT VS. FORWARD VOLTAGE



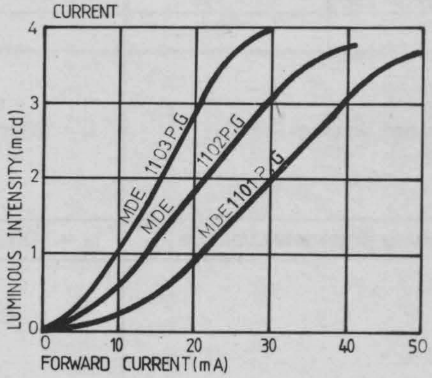
RELATIVE LUMINOUS INTENSITY VS ANGULAR DISPLACEMENT



LUMINOUS INTENSITY VS. FORWARD CURRENT



LUMINOUS INTENSITY VS. FORWARD CURRENT



RECTANGULAR LIGHT EMITTING DIODES

GENERAL DESCRIPTION

The MDE 1531...3R (P, G or V) are visible sources (red, amber, yellow or green) using a planar technology $GaAs_{1-x}P_x$ (x = 0...1)
They utilise a tinted, diffused expoxy to provide high contrast and a flat high intensity emitting surface; bordeless package design allows creation of uninterrupted light emitting areas.

FEATURES

- High Luminous Intensity
- Rectangular Light Emitting surface
- Long Life
- IC Compatible
- Low Current Requirements

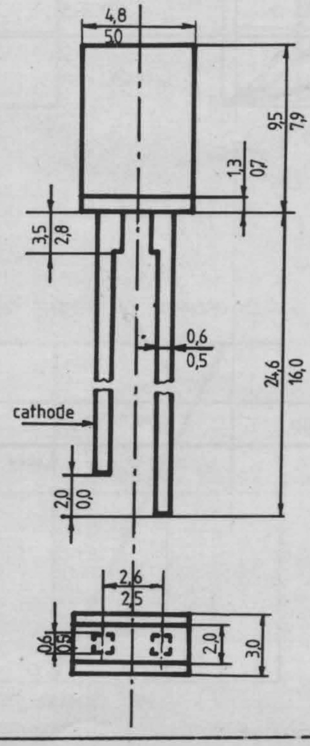
APPLICATIONS

- Flush Mounted Panel Indicators
- Backlighting Legends
- Bar graph Display

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	VALUES	UNIT
I_{Fmax}	DC Forward Current	50	mA
$I_{Fpeak\ max}$	Peak Forward Current (1 μsec pulse width, 300 pps)	1	A
P_{dmax}	DC Power Dissipation	150	mW
T_A	Operating Temperature	0...+70	°C
T_{stg}	Storage Temperature	−40...+85	°C
T_{ead}	Lead Soldering Temperature	+260	°C

PACKAGE DIMENSIONS



OPTOELECTRONIC CHARACTERISTICS AT $T_A = 25°C$

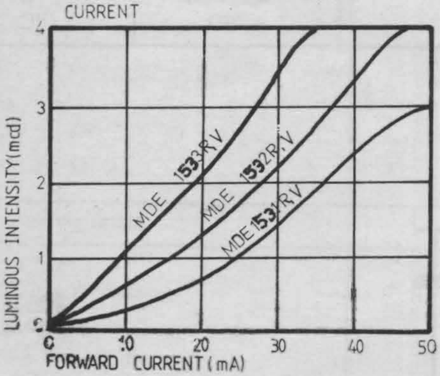
PARAMETER		TEST CONDITIONS	DEVICE	VALUES		UNIT
				min.	max.	
I_V	Luminous Intensity	$I_F = 20$ mA	MDE 1531R MDE 1531V	0.1	1	mcd
			MDE 1532R MDE 1532V	1	2	mcd
			MDE 1533R MDE 1533V	2		mcd
			MDE 1531P MDE 1531G	0.3	1.5	mcd
			MDE 1532P MDE 1532G	1.5	2.5	mcd
			MDE 1533P MDE 1533G	2.5		mcd
λ_p	Peak Wavelength	$I_F = 20$ mA	MDE 1531R MDE 1532R MDE 1533R	645	680	nm
			MDE 1531P MDE 1532P MDE 1533P	625	640	nm
			MDE 1531G MDE 1532G MDE 1533G	573	590	nm
			MDE 1531V MDE 1532V MDE 1533V	554	570	nm
$\theta_{1/2}$	Viewing Angle	$I_F = 20$ mA			40	grad
V_F	Forward Voltage	$I_F = 20$ mA	MDE 1531R MDE 1532R MDE 1533R		2	V
			MDE 1531P MDE 1532P MDE 1533P MDE 1531G MDE 1532G MDE 1533G MDE 1531V MDE 1532V MDE 1533V		3	V
BV_R	Reverse Breakdown Voltage I	$I_R = 100\ \mu A$		3		V
Co	Capacitance	$V_F = 0$ V, f = 1 MHz	MDE 1531R MDE 1532R MDE 1533R		70	pF

OPTOELECTRONIC CHARACTERISTICS AT $T_A = 25°C$

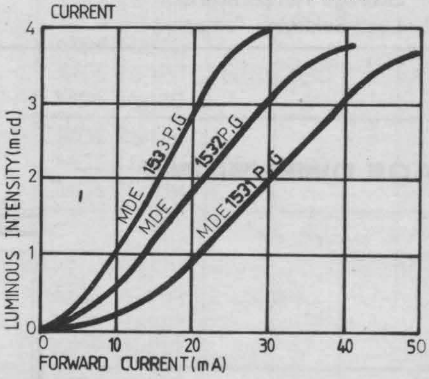
PARAMETER	TEST CONDITIONS	DEVICE	VALUES min.	VALUES max.	UNIT
		MDE 1531P MDE 1532P MDE 1533P MDE 1531G MDE 1532G MDE 1533G MDE 1531V MDE 1532V MDE 1533V		60	pF

Note: R — red
V — green
G — yellow
P — amber

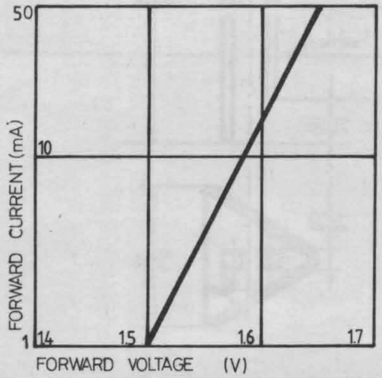
LUMINOUS INTENSITY VS. FORWARD CURRENT



LUMINOUS INTENSITY VS. FORWARD CURRENT



FORWARD CURRENT VS. FORWARD VOLTAGE



TRIANGULAR LIGHT EMITTING DIODES

GENERAL DESCRIPTION

The MDE 1541...3R (P, G or V) are visible sources (red, amber, yellow or green) using a planar technology $GaAs_{1-x}P_x$ ($x = 0...1$)
They utilise a tinted, diffused expoxy to provide high contrast and a flat high intensity emitting surface; bordeless package design allows creation of uninterrupted light emitting areas.

FEATURES

- High Intensity
- Rectangular Light Emitting surface
- Long Life
- IC Compatible
- Low Current Requirements

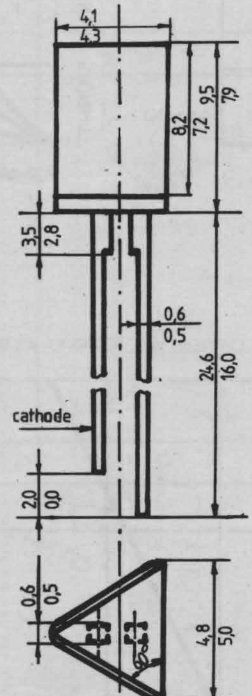
APPLICATIONS

- Light Indicators

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	VALUES	UNIT
I_{Fmax}	DC Forward Current	50	mA
$I_{Fpeak\ max}$	Peak Forward Current (1 μsec pulse width, 300 pps)	1	A
P_{dmax}	DC Power Dissipation	150	mW
T_A	Operating Temperature	0...+70	°C
T_{stg}	Storage Temperature	−40...+85	°C
T_{ead}	Lead Soldering Temperature	+260	°C

PACKAGE DIMENSIONS



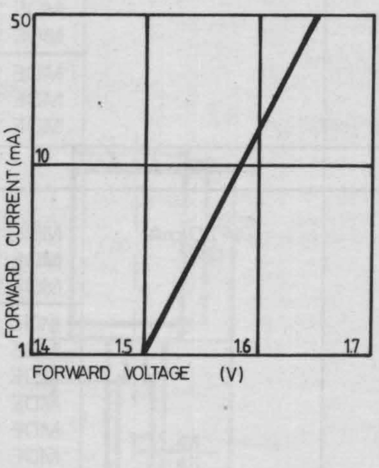
OPTOELECTRONIC CHARACTERISTICS AT $T_A = 25°C$

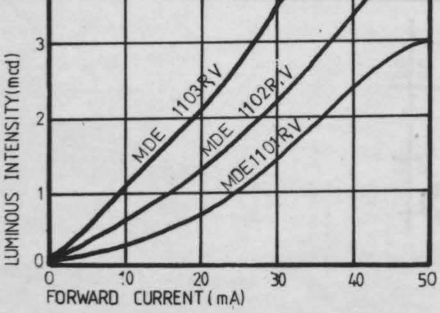
PARAMETER		TEST CONDITIONS	DEVICE	VALUES		UNIT
				min.	max.	
I_V	Luminous Intensity	$I_F = 20$ mA	MDE 1541R MDE 1541V	0.1	1	mcd
			MDE 1542R MDE 1542V	1	2	mcd
			MDE 1543R MDE 1543V	2		mcd
			MDE 1541P MDE 1541G	0.3	1.5	mcd
			MDE 1542P MDE 1542G	1.5	2.5	mcd
			MDE 1543P MDE 1543G	2.5		mcd
λ_p	Peak Wavelength	$I_F = 20$ mA	MDE 1541R MDE 1542R MDE 1543R	645	680	nm
			MDE 1541P MDE 1542P MDE 1543P	625	640	nm
			MDE 1541G MDE 1542G MDE 1543G	573	590	nm
			MDE 1541V MDE 1542V MDE 1543V	554	570	nm
$\theta_{1/2}$	Viewing Angle	$I_F = 20$ mA			40	grad
V_F	Forward Voltage	$I_F = 20$ mA	MDE 1541R MDE 1542R MDE 1543R		2	V
			MDE 1541P MDE 1542P MDE 1543P MDE 1541G MDE 1542G MDE 1543G MDE 1541V MDE 1542V MDE 1543V		3	V

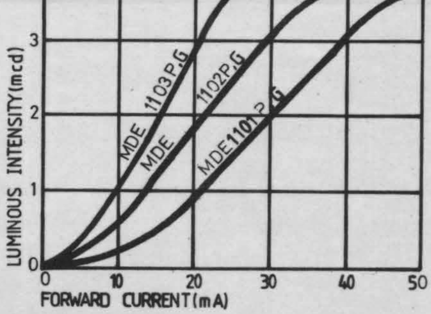
OPTOELECTRONIC CHARACTERISTICS AT $T_A = 25°C$

PARAMETER	TEST CONDITIONS	DEVICE	VALUES min.	VALUES max.	UNIT
BV_R Reverse Breakdown Voltage	$I_R = 100\ \mu A$		3		V
Co Capacitance	$V_F = 0\ V$, f = 1 MHz	MDE 1541R MDE 1542R MDE 1543R		70	pF
		MDE 1541P MDE 1542P MDE 1543P MDE 1541G MDE 1542G MDE 1543G MDE 1541V MDE 1542V MDE 1543V		60	pF

Note: R — red
V — green
G — yellow
P — amber







RESISTOR LED S

GENERAL DESCRIPTIONS

The resistor LED S (5 V/16 mA) are visible sources (red, amber, yellow or green) with epoxy lens
The LED are using $GaAs_{1-x}P_x$ (x = 0...1) and resistive silicon chips.

FEATURES

- TTL Compatibile
- Integral Current Limiting Rezistor
- Rugged and Reliable

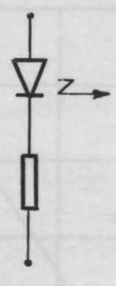
APPLICATIONS

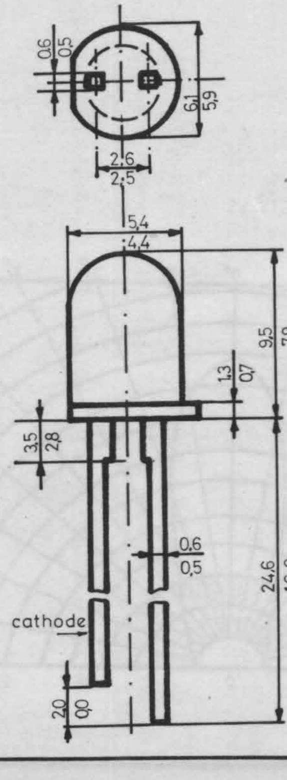
- Use in TTL circuits

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	VALUES	UNIT
V_{Fmax}	DC Forward Voltage	7	V
V_{Rmax}	Reverse Voltage	7	V
P_{dmax}	DC Power Dissipation	180.	mW
I_{Fmax}	DC Forward Current	25.	mA
T_A	Operating Temperature	0...+70	°C
T_{stg}	Storage Temperature	−40...+85	°C
T_{sol}	Lead Soldering Temperature	+260	°C

PACKAGE DIMENSIONS



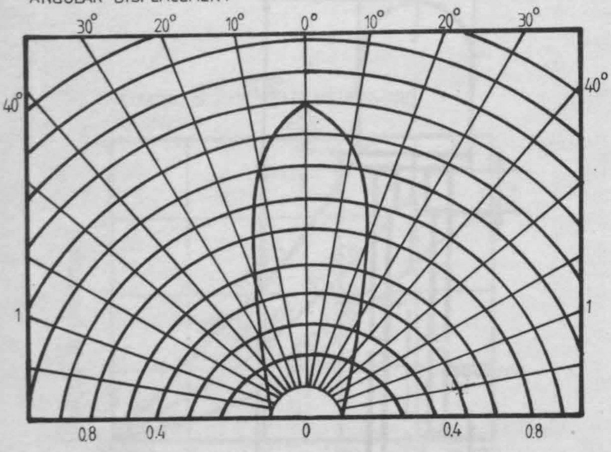


OPTOELECTRIC CHARACTERISTICS AT $T_A = 25°C$

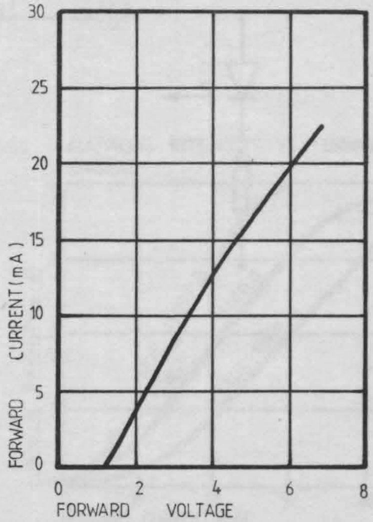
PARAMETER	TEST CONDITIONS	DEVICE	min.	max.	UNIT
I_F Forward Current	$V_F = 5$ V		14	20	mA
I_V Luminous Intensity	$V_F = 5$ V	MDE 1601R, MDE 1601V	0.3	1	mcd
		MDE 1602R, MDE 1602V	1	2	mcd
		MDE 1603R, MDE 1603V	2		mcd
		MDE 1601P, MDE 1601G	0.3	1.5	mcd
		MDE 1602P, MDE 1602G	1.5	2.5	mcd
		MDE 1603P, MDE 1603G	2.5		mcd
λ_P Peak Wavelength	$I_F = 16$ mA	MDE 1601P, MDE 1602P MDE 1603P,	625	640	nm
		MDE 1601G, MDE 1602G MDE 1603G,	573	590	nm
		MDE 1601V, MDE 1602V MDE 1603V	554	570	nm
		MDE 1601R, MDE 1602R MDE 1603R	645	680	nm
$\theta_{1/2}$ Viewing Angle	$I_F = 16$ mA		40		grad
BV_R Reverse Breakdown Voltage	$I_R = 100\ \mu A$		5		V
C_D Capacitance	$V_F = 0$ V f = 1 MHz	MDE 1601R, MDE 1602R MDE 1603R, MDE 1601P, MDE 1602P MDE 1603P,		70	pF
		MDE 1601G, MDE 1602G MDE 1603G MDE 1601V, MDE 1602V MDE 1603V		60	pF

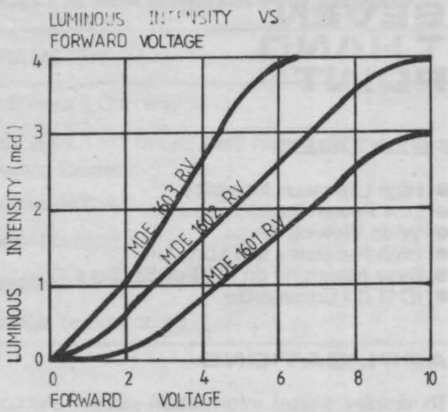
Note: R — red
V — green
G — yellow
P — amber

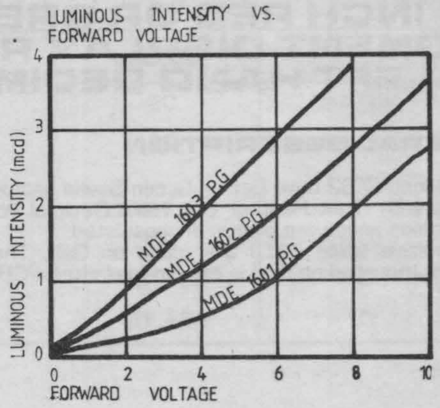
RELATIVE LUMINOUS INTENSITY VS.
ANGULAR DISPLACEMENT



FORWARD CURRENT VS
FORWARD VOLTAGE




LUMINOUS INTENSITY VS
FORWARD VOLTAGE
LUMINOUS INTENSITY (mcd)
FORWARD VOLTAGE
MDE 1603 RV
MDE 1602 RV
MDE 1601 RV
0
1
2
3
4
0
2
4
6
8
10


LUMINOUS INTENSITY VS.
FORWARD VOLTAGE
LUMINOUS INTENSITY (mcd)
FORWARD VOLTAGE
MDE 1603 PG
MDE 1602 PG
MDE 1601 PG
0
1
2
3
4
0
2
4
6
8
10

0.3 INCH RED OR GREEN SEVEN SEGMENT DISPLAY RIGHT HAND OR LEFT HAND DECIMAL POINT

GENERAL DESCRIPTION

The 0.3 Inch (7.62 mm) Red or Green Seven segment Displays with Right Hand or Left Hand Decimal Point and common anode are plastic encapsulated.
The emissive chips (LED) are made on GaP. These chips are mounted on dual in line pin-implanted. PCB s.

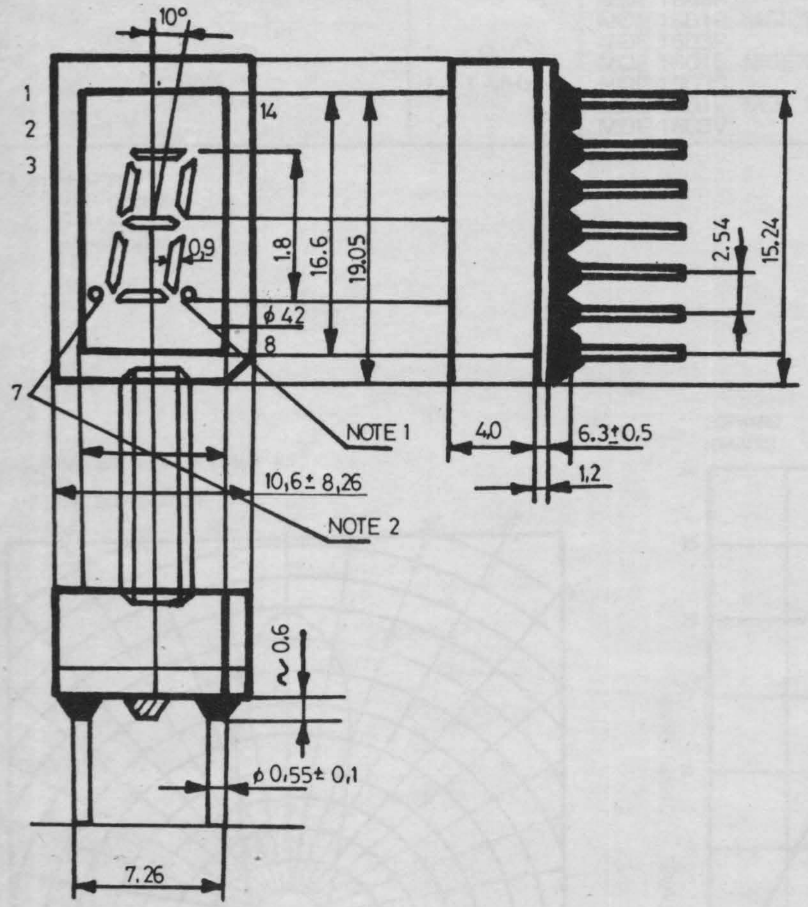
FEATURES

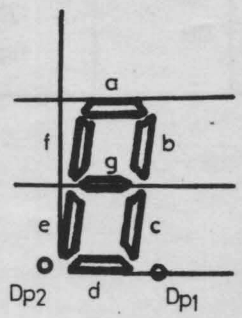
- High Luminous Intensity
- Low Power Requirements
- Wide Viewing Angle
- High Reliability and Long Life
- Easy Mounting on PCB or Sockets
- IC (TTL) Compatible

APPLICATIONS

To display digital information used in electrical equipments where it is neccessary.

PACKAGE DIMENSIONS





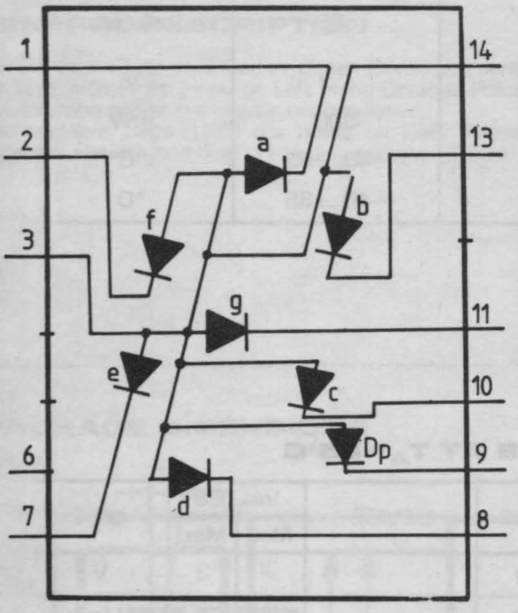
ABSOLUTE MAXIMUM RATINGS

	PARAMETER	VALUES	UNIT
I_F	DC Forward Current	20	mA/seg
I_{FP}	Pulse (width = 1 msec, duty ratio = 25%) Forward Current	60	mA/seg
V_R	Reverse Voltage	3	V
P_D	Power Dissipation	300	mW
T_A	Operating Temperature	−40...+85	°C
T_{stg}	Storage Temperature	−40...+85	°C

OPTOELECTRONIC CHARACTERISTICS AT $T_A = 25°C$

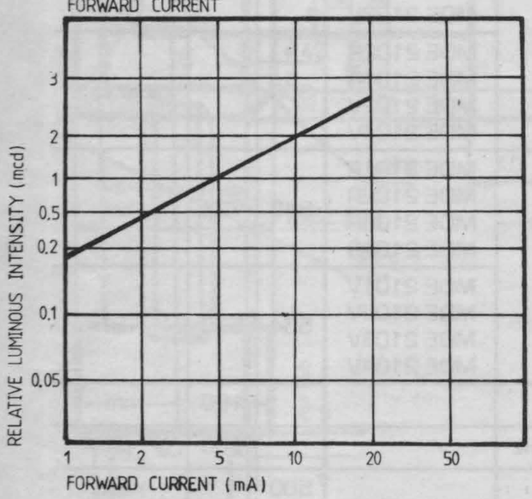
	PARAMETER	TEST CONDITIONS	DEVICE	VALUES Min.	VALUES Max.	UNIT
V_F	Forward Voltage	I_F = 10 mA/seg			3	V
V_R	Reverse Breakdown Voltage	I_R = 100 μA/seg		3		V/seg
I_V	Luminous Intensity	I_F = 10 mA/seg	MDE 2101R MDE 2103R MDE 2101V MDE 2103V	180		μcd/seg
			MDE 2102R MDE 2104R MDE 2102V MDE 2104V	300		μcd/seg
λ_p	Emission Peak Wavelength	I_F = 10 mA/seg	MDE 2101R MDE 2102R MDE 2103R MDE 2104R	645	725	nm
			MDE 2101V MDE 2102V MDE 2103V MDE 2104V	554	570	nm
$\Delta\lambda$	Line Half Width	I_F = 10 mA/seg			100	nm
Co	Capacitance	V_F = 0 V, f = 1 MHz			200	pF
t	Response Time			500		nsec

CONNECTION DIAGRAM

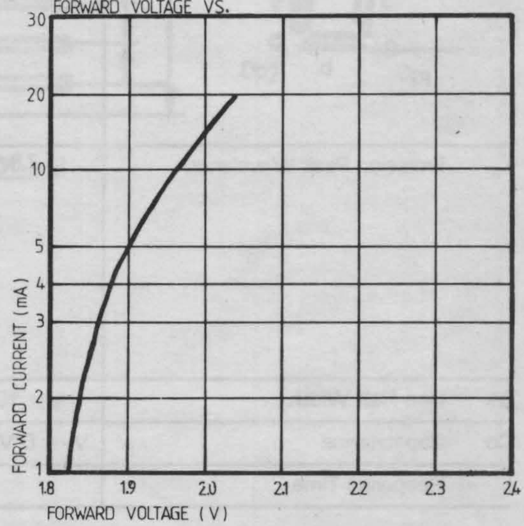


PIN. NO.	ADDRESS	PIN. NO.	ADDRESS
1.	a CATHODE	8.	d CATHODE
2.	f CATHODE	9.	D.p CATHODE
3.	COMMON ANODE	10.	c CATHODE
4.	NO PIN	11.	g CATHODE
5.	NO PIN	12.	NO PIN
6.	NO PIN	13.	b CATHODE
7.	e CATHODE	14.	COMMON ANODE

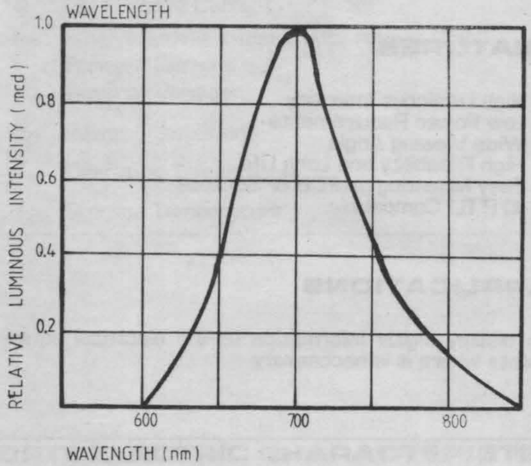
LUMINOUS INTENSITY VS.
FORWARD CURRENT



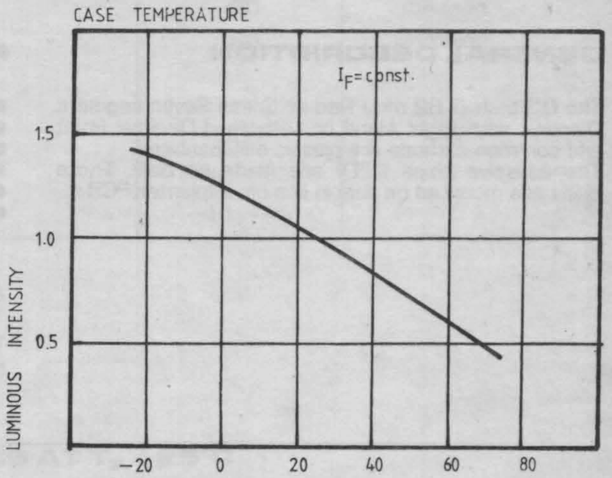
FORWARD CURRENT
FORWARD VOLTAGE VS.



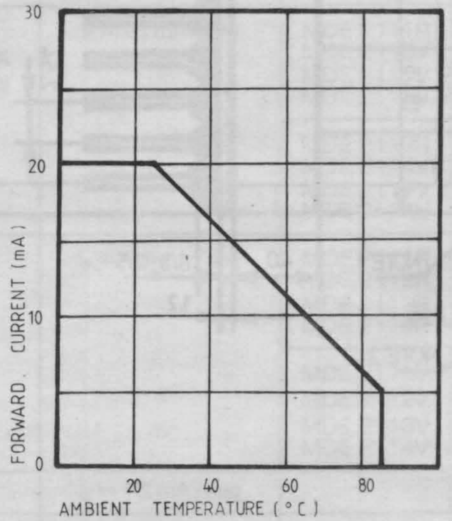
RELATIVE LUMINOUS INTENSITY VS. WAVELENGTH



LUMINOUS INTENSITY VS. CASE TEMPERATURE



FORWARD CURRENT VS. AMBIENT TEMPERATURE



0.3 INCH RED OR GREEN SEVEN SEGMENT DISPLAY RIGHT HAND OR LEFT HAND DECIMAL POINT

GENERAL DESCRIPTION

The 0.3 Inch (7.62 mm) Red or Green Seven segment Displays with Right Hand or Left Hand Decimal Point and common cathode are plastic encapsulated.
The emissive chips (LED) are made on GaP. These chips are mounted on dual in line pin-implanted.PCB s.

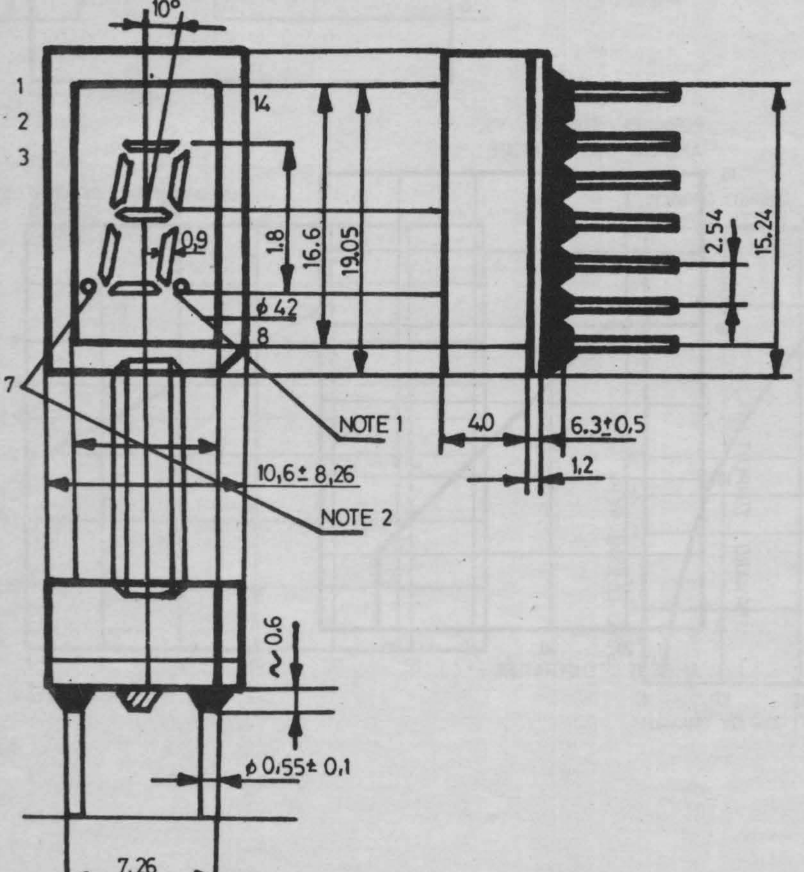
FEATURES

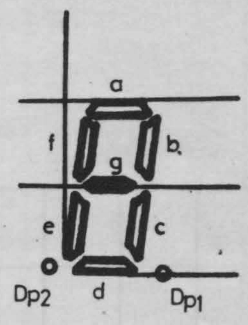
- High Luminous Intensity
- Low Power Requirements
- Wide Viewing Angle
- High Reliability and Long Life
- Easy Mounting on PCB or Sockets
- IC (TTL) Compatible

APPLICATIONS

To display digital information used in electrical equipments where it is neccessary.

PACKAGE DIMENSIONS





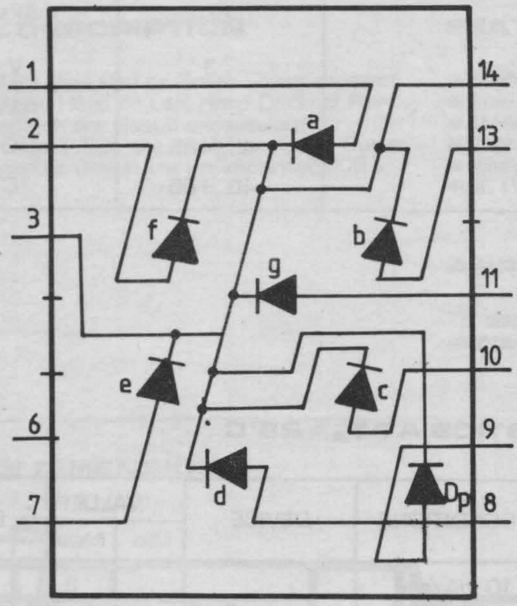
ABSOLUTE MAXIMUM RATINGS

	PARAMETER	VALUES	UNIT
I_F	DC Forward Current	20	mA/seg
I_{FP}	Pulse (width = 1 msec, duty ratio = 25%) Forward Current	60	mA/seg
V_R	Reverse Voltage	3	V
P_D	Power Dissipation	300	mW
T_A	Operating Temperature	−40...+85	°C
T_{stg}	Storage Temperature	−40...+85	°C

OPTOELECTRIC CHARACTERISTICS AT $T_A = 25°C$

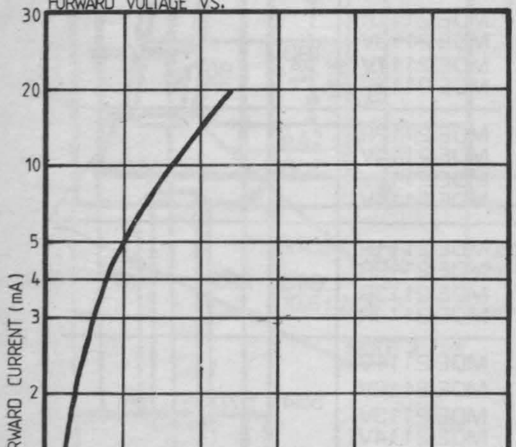
	PARAMETER	TEST CONDITIONS	DEVICE	VALUES Min.	VALUES Max.	UNIT
V_F	Forward Voltage	I_F = 10 mA/seg			3	V
V_R	Reverse Breakdown Voltage	I_R = 100 μA/seg		3		V/seg
I_V	Luminous Intensity	I_F =10 mA/seg	MDE 2111R MDE 2113V MDE 2111V MDE 2113V	180		μcd/seg
			MDE 2112R MDE 2114V MDE 2112V MDE 2114V	.300		μcd/seg
λ_p	Emission Peak Wavelength	I_F = 10 mA/seg	MDE 2111R MDE 2112R MDE 2113R MDE 2114R	645	725	nm
			MDE 2111V MDE 2112V MDE 2113V MDE 2114V	554	570	nm
$\Delta\lambda$	Line Half Width	I_F = 10 mA/seg			100	nm
Co	Capacitance	V_F = 0V f = 1 MHz			200	pF
t	Response Time			500		nsec

CONNECTION DIAGRAM

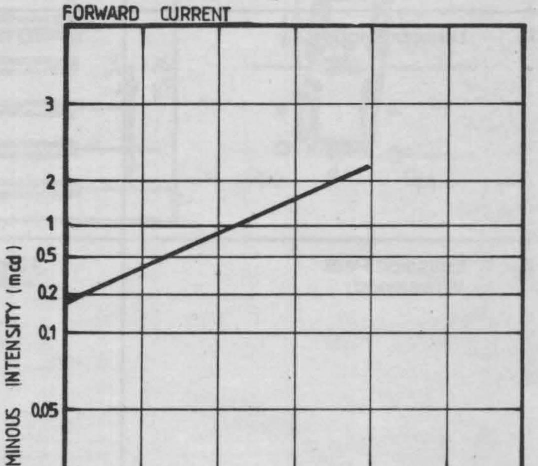


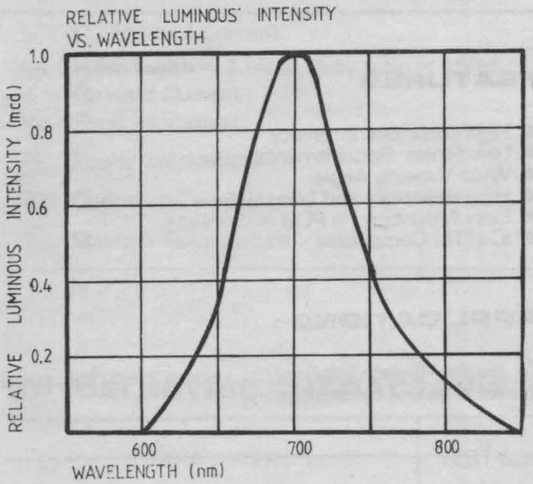
PIN NO	ADDRESS	PIN NO	ADDRESS
1	a ANODE	8	d ANODE
2	f ANODE	9	D.p ANODE
3	COMMON CATHODE	10	c ANODE
4	NO PIN	11	g ANODE
5	NO PIN	12	NO PIN
6	NO PIN	13	b ANODE
7	e ANODE	14	COMMON CATHODE

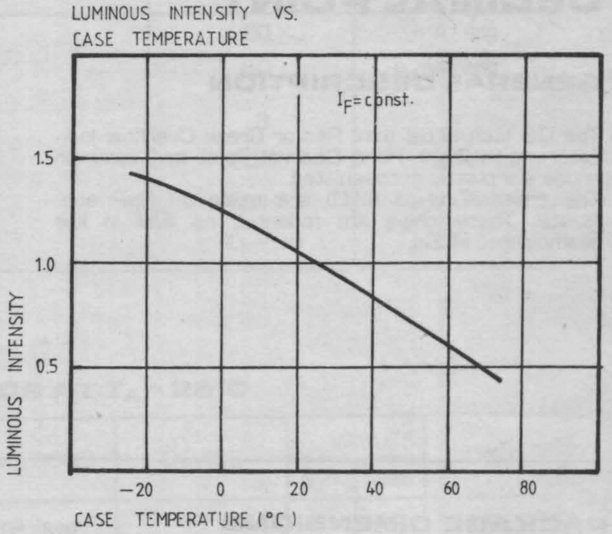
FORWARD CURRENT
FORWARD VOLTAGE VS.

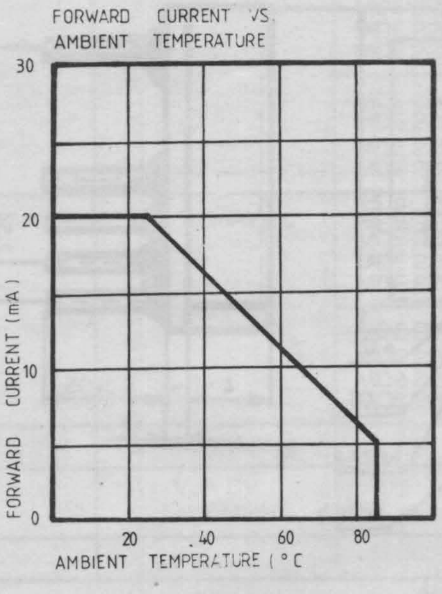


LUMINOUS INTENSITY VS
FORWARD CURRENT




RELATIVE LUMINOUS INTENSITY
VS. WAVELENGTH
RELATIVE LUMINOUS INTENSITY (mcd)
1.0
0.8
0.6
0.4
0.2
600
700
800
WAVELENGTH (nm)


LUMINOUS INTENSITY VS.
CASE TEMPERATURE
I_F= const.
LUMINOUS INTENSITY
1.5
1.0
0.5
−20
0
20
40
60
80
CASE TEMPERATURE (°C)


FORWARD CURRENT VS.
AMBIENT TEMPERATURE
FORWARD CURRENT (mA)
30
20
10
0
20
40
60
80
AMBIENT TEMPERATURE (°C

0.3 INCH RED OR GREEN OVERFLOW INDICATOR RIGHT HAND OR LEFT HAND DECIMAL POINT

GENERAL DESCRIPTION

The 0.3 Inch (7.62 mm) Red or Green Overflow Indicators with Right Hand Decimal Point and common anode are plastic encapsulated.
The emissive chips (LED) are made on GaP substrate. These chips are mounted on dual in line pinimplanted PCBs.

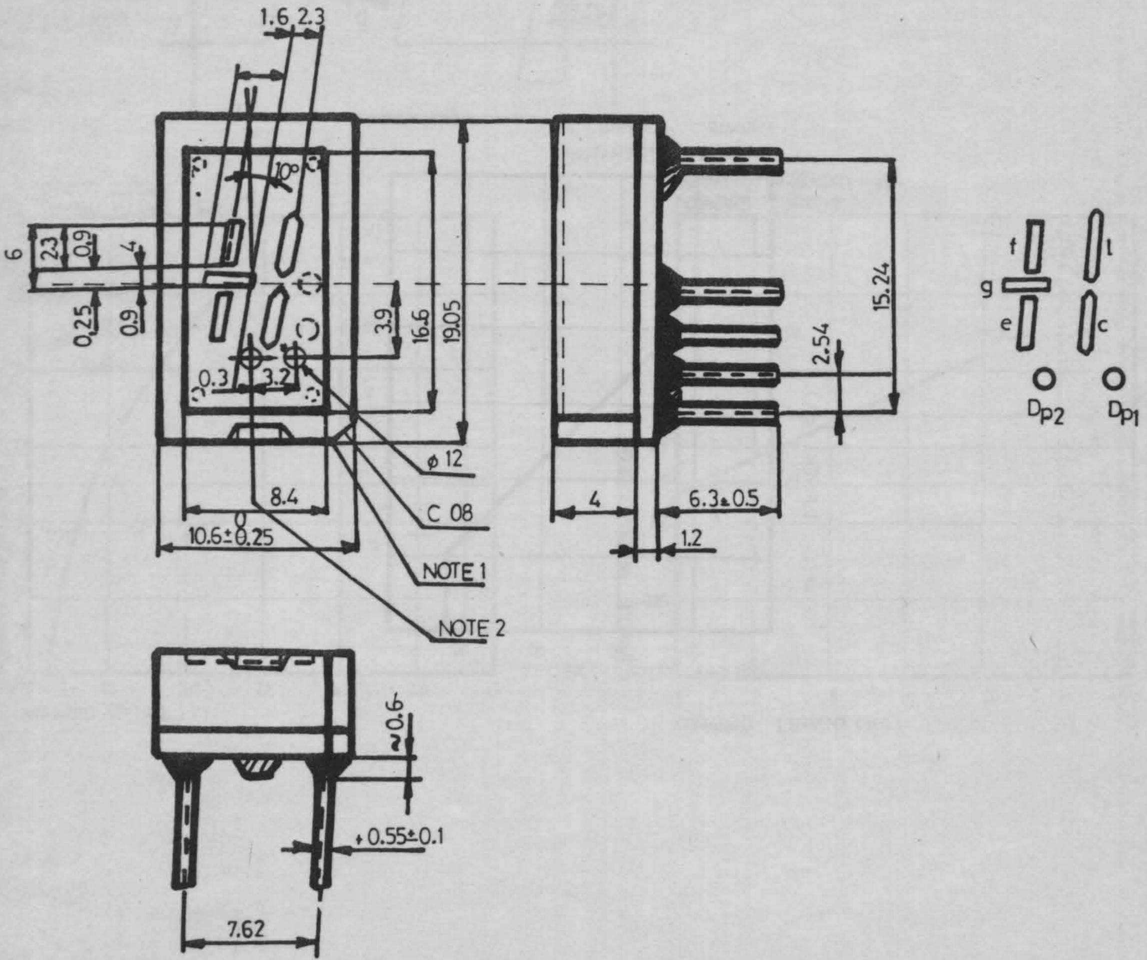
FEATURES

- High Luminous Intensity
- Low Power Requirements
- Wide Viewing Angle
- High Reliability and Long Life
- Easy Mounting on PCB or Sockets
- IC (TTL) Compatible

APPLICATIONS

To display digital information used in electrical equipments where it is neccessary.

PACKAGE DIMENSIONS



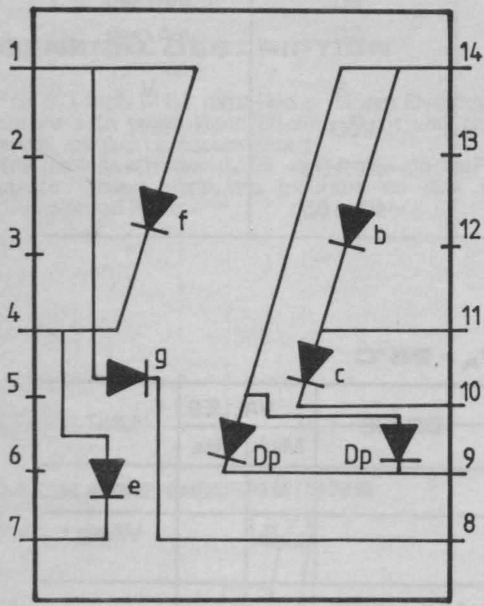
ABSOLUTE MAXIMUM RATINGS

	PARAMETER	VALUES	UNIT
I_F	DC Forward Current	20	mA/seg
I_{FP}	Pulse (width = 1 msec, duty ratio ≦ 25%) Forward Current	60	mA/seg
V_R	Reverse Voltage	3	V
P_D	Power Dissipation	200	mW
T_A	Operating Temperature	−40...+85	°C
T_{stg}	Storage Temperature	−40...+85	°C

OPTOELECTRIC CHARACTERISTICS AT $T_A = 25°C$

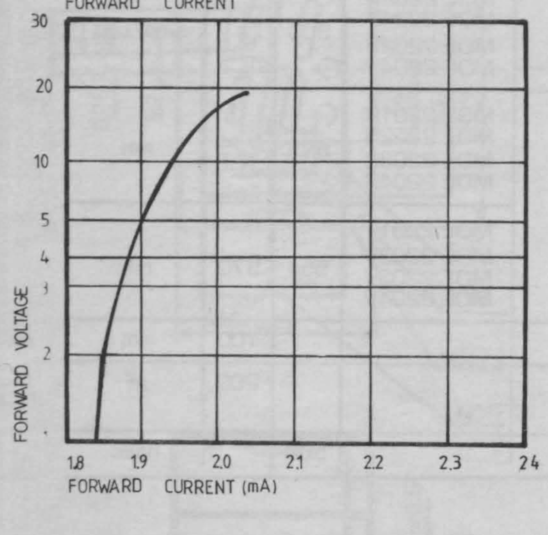
	PARAMETER	TEST CONDITIONS	DEVICE	VALUES		UNIT
				Min.	Max.	
V_F	Forward Voltage	$I_F = 10$ mA/seg			3	V
V_R	Reverse Breakdown Voltage	$I_R = 100$ μA/seg		3		V/seg
I_V	Luminous Intensity	$I_F = 10$ mA/seg	MDE 2201R MDE 2203V MDE 2201V MDE 2203V	180		μcd/seg
			MDE 2202R MDE 2204V MDE 2202V MDE 2204V	300		μcd/seg
λ_p	Emission Peak Wavelength	$I_F = 10$ mA/seg	MDE 2201R MDE 2202R MDE 2203R MDE 2204R	645	725	nm
			MDE 2201V MDE 2202V MDE 2203V MDE 2204V	554	570	nm
$\Delta\lambda$	Line Half Width	$I_F = 10$ mA/seg			100	nm
Co	Capacitance	$V_F = 0V$ f = 1 MHz			200	pF
t	Response Time			500		nsec

CONNECTION DIAGRAM

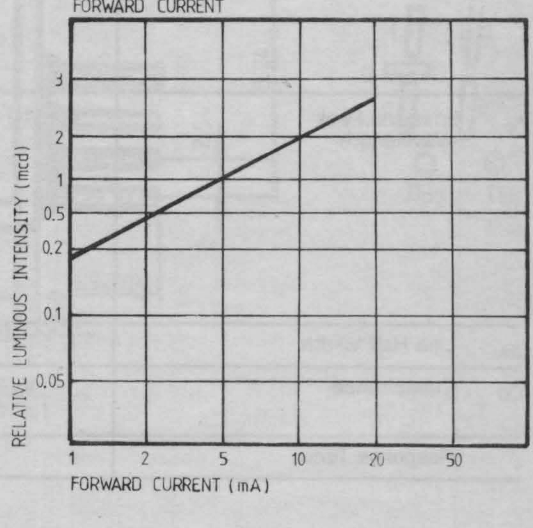


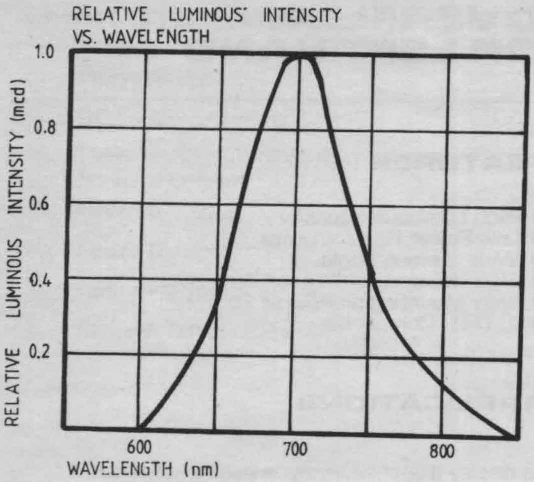
PIN. NO.	ADDRESS	PIN. NO.	ADDRESS
1.	f,g ANODE	8.	g CATHODE
2.	NO PIN	9.	D.p CATHODE
3.	NO PIN	10.	c CATHODE
4.	e ANODE, f CATHODE	11.	b CATODE c ANODE
5.	NO PIN	12.	NO PIN
6.	NO PIN	13.	NO PIN
7.	e CATHODE	14.	b,D.p ANODE

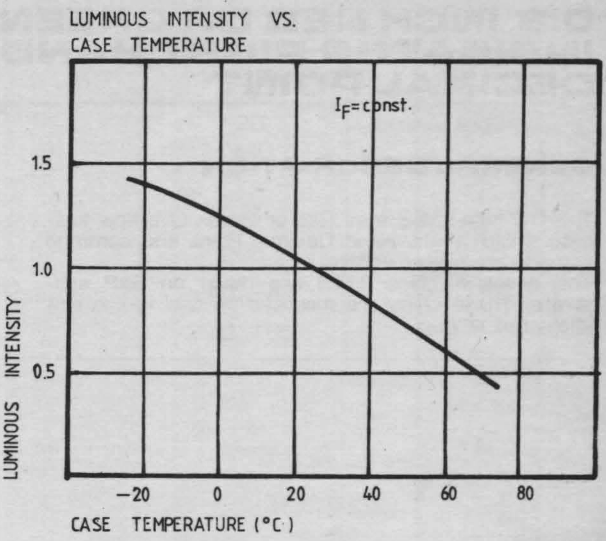
FORWARD VOLTAGE VS FORWARD CURRENT

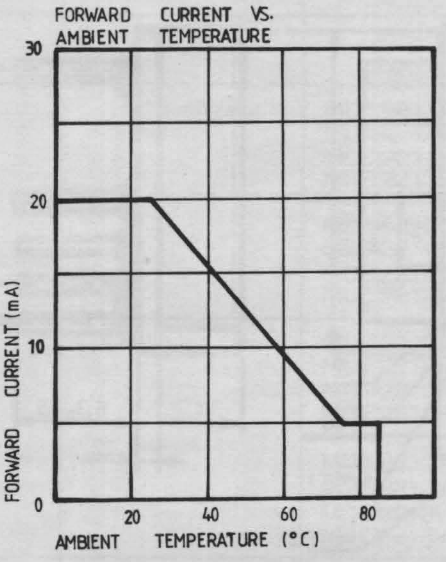


LUMINOUS INTENSITY VS. FORWARD CURRENT




RELATIVE LUMINOUS INTENSITY
VS. WAVELENGTH
RELATIVE LUMINOUS INTENSITY (mcd)
1.0
0.8
0.6
0.4
0.2
600
700
800
WAVELENGTH (nm)


LUMINOUS INTENSITY VS.
CASE TEMPERATURE
I_F=const.
LUMINOUS INTENSITY
1.5
1.0
0.5
−20
0
20
40
60
80
CASE TEMPERATURE (°C)


FORWARD CURRENT VS.
AMBIENT TEMPERATURE
FORWARD CURRENT (mA)
30
20
10
0
20
40
60
80
AMBIENT TEMPERATURE (°C)

0.3 INCH RED OR GREEN OVERFLOW INDICATOR RIGHT HAND OR LEFT HAND DECIMAL POINT

GENERAL DESCRIPTION

The 0.3 Inch (7.62 mm) Red or Green Overflow Indicators with Right Hand Decimal Point and common cathode are plastic encapsulated.
The emissive chips (LED) are made on GaP substrate. These chips are mounted on dual in line pin-implanted PCB s.

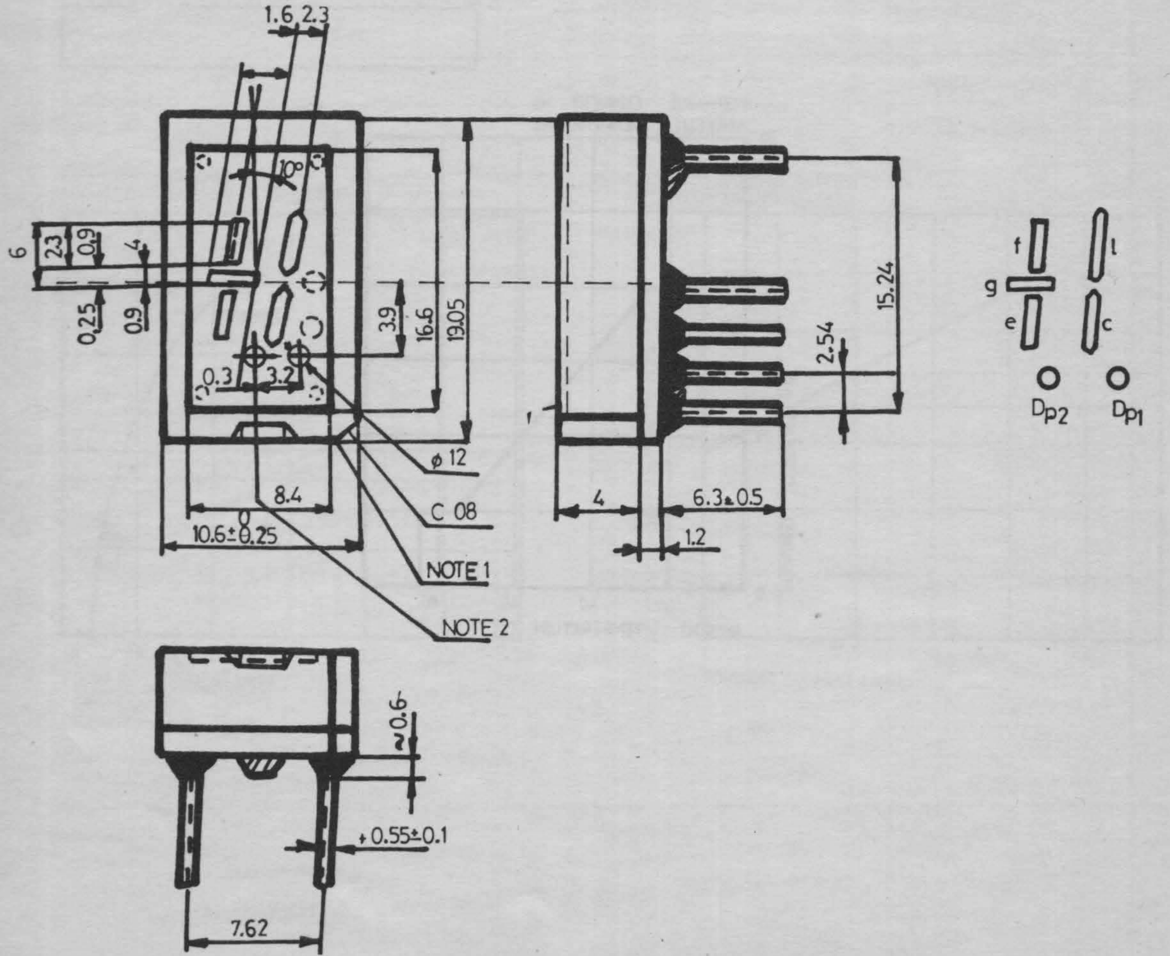
FEATURES

- High Luminous Intensity
- Low Power Requirements
- Wide Viewing Angle
- High Reliability and Long Life
- Easy Mounting on PCB or Sockets
- IC (TTL) Compatible

APPLICATIONS

To display digital information used in electrical equipments where it is neccessary.

PACKAGE DIMENSIONS



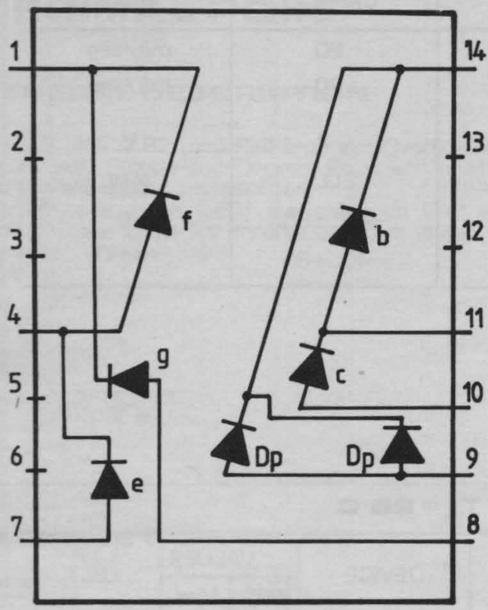
ABSOLUTE MAXIMUM RATINGS

	PARAMETER	VALUES	UNIT
I_F	DC Forward Current	20	mA/seg
I_{FP}	Pulse (width = 1 msec, duty ratio = 25%) Forward Current	60	mA/seg
V_R	Reverse Voltage	3	V
P_D	Power Dissipation	200	mW
T_A	Operating Temperature	−40...+85	°C
T_{stg}	Storage Temperature	−40...+85	°C

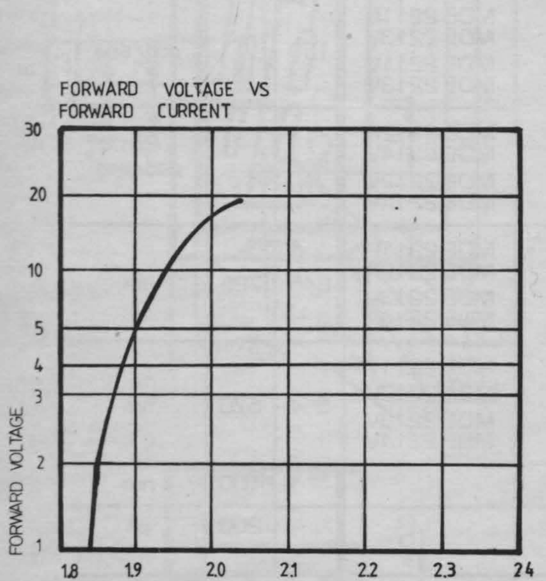
OPTOELECTRIC CHARACTERISTICS AT $T_A = 25°C$

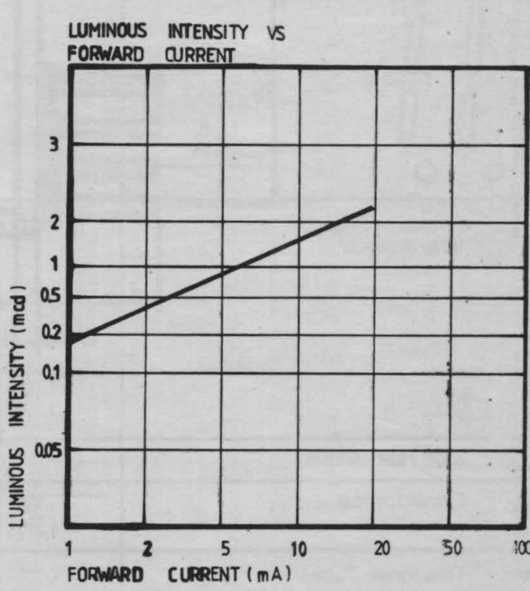
	PARAMETER	TEST CONDITIONS	DEVICE	VALUES Min.	VALUES Max.	UNIT
V_F	Forward Voltage	I_F = 10 mA/seg			3	V
V_R	Reverse Breakdown Voltage	I_R = 100 μA/seg		3		V/seg
I_V	Luminous Intensity	I_F =10 mA/seg	MDE 2211R MDE 2213V MDE 2211V MDE 2213V	180		μcd/seg
			MDE 2212R MDE 2214V MDE 2212V MDE 2214V	300		μcd/seg
λ_p	Emission Peak Wavelength	I_F = 10 mA/seg	MDE 2211R MDE 2212R MDE 2213R MDE 2214R	645	725	nm
			MDE 2211V MDE 2212V MDE 2213V MDE 2214V	554	570	nm
$\Delta\lambda$	Line Half Width	I_F = 10 mA/seg			100	nm
Co	Capacitance	V_F = 0V f = 1 MHz			200	pF
t	Response Time			500		nsec

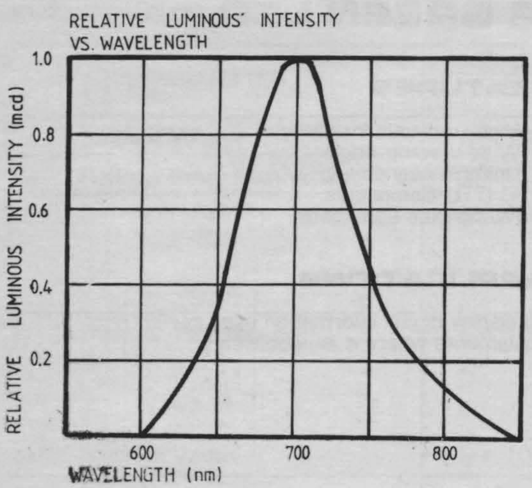
FUNCTIONAL DIAGRAM

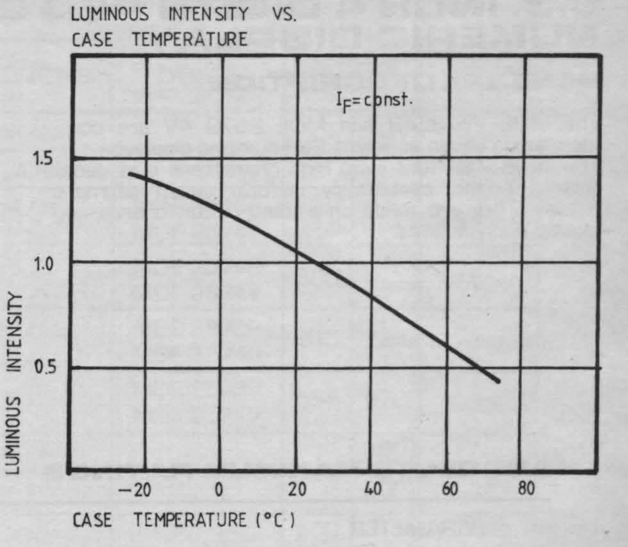


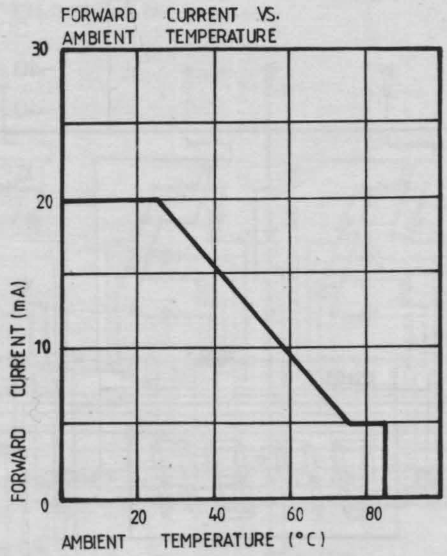
PIN NO	ADDRESS	PIN NO	ADDRESS
1	f,g CATHODE	8	g ANODE
2	NO PIN	9	D.p ANODE
3	NO PIN	10	c ANODE
4	e CATHODE f ANODE	11	b ANODE c CATHODE
5	NO PIN	12	NO PIN
6	NO PIN	13	NO PIN
7	e ANODE	14	b,D.p CATHODE






RELATIVE LUMINOUS INTENSITY
VS. WAVELENGTH
RELATIVE LUMINOUS INTENSITY (mcd)
1.0
0.8
0.6
0.4
0.2
600
700
800
WAVELENGTH (nm)


LUMINOUS INTENSITY VS.
CASE TEMPERATURE
I_F=const.
LUMINOUS INTENSITY
1.5
1.0
0.5
−20
0
20
40
60
80
CASE TEMPERATURE (°C)


FORWARD CURRENT VS.
AMBIENT TEMPERATURE
FORWARD CURRENT (mA)
30
20
10
0
20
40
60
80
AMBIENT TEMPERATURE (°C)

0.3. INCH 4 DIGITS RED OR GREEN LED NUMERIC DISPLAY

GENERAL DESCRIPTION

The MDE 2573...4R and MDE 2573...4V are common anode seven segment GaP numeric displays.
The large 7.62 (0.3 inch) high characters size generate a bright, continously uniform seven segment display. They are made on printed circuit boards and plastic encapsulated.

FEATURES

- High Luminous Intensity
- Wide Viewing Angle
- Uniform Alignement
- IC (TTL) Compatible
- Multiplexed adressable

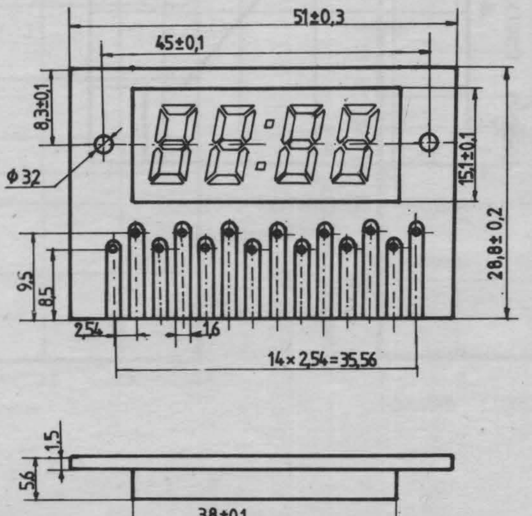
APPLICATIONS

To display digital information used in electrical equipments where it is neccessary.

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	VALUES	UNIT
I_F	DC Forward Current	20	mA/seg
I_{FP}	Pulse (width =1 msec, duty ratio = 25%) Forward Current	60	mA/seg
V_R	Reverse Voltage	3	V
P_D	Power Dissipation	300	mW
T_A	Operating Temperature	−40...+85	°C
T_{stg}	Storage Temperature	−40...+85	°C

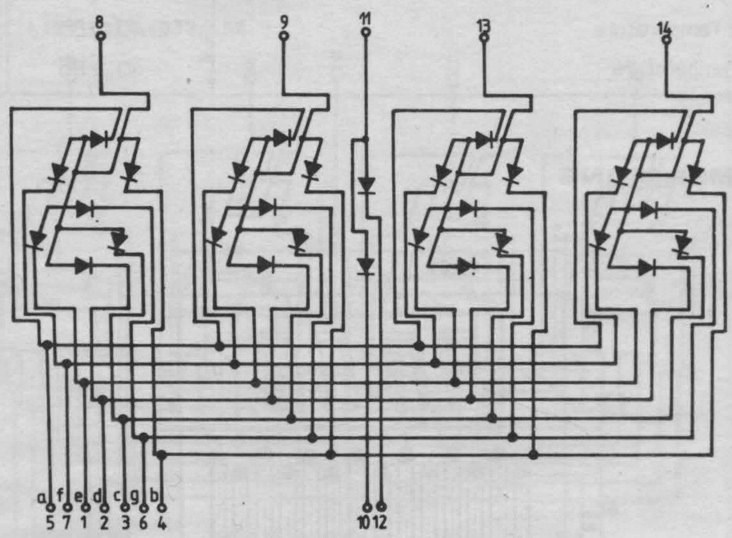
PACKAGE DIMENSIONS



OPTOELECTRONIC CHARACTERISTICS AT $T_A = 25°C$

PARAMETER		TEST CONDITIONS	DEVICE	VALUES		UNIT
				Min.	Max.	
V_F	Forward Voltage	$I_F = 10$ mA/seg		1.9	3	V
V_R	Reverse Breakdown Voltage	$I_R = 100$ μA/seg		3		V/seg
I_V	Luminous Intensity	$I_F = 10$ mA/seg	MDE 2573R MDE 2574V	180		μcd/seg
			MDE 2574R MDE 2574V	300		μcd/seg
λ_p	Emission Peak Wavelength	$I_F = 10$ mA/seg	MDE 2573R MDE 2574R	645	725	nm
			MDE 2573V MDE 2574V	554	570	nm
$\Delta\lambda$	Line Half Width	$I_F = 10$ mA/seg			100	nm
Co	Capacitance	$V_F = 0V$, f = 1 MHz			200	pF
t	Response Time			500		nsec

INTERNAL CIRCUIT DIAGRAM



PIN	FUNCTION	PIN	FUNCTION
1	e Cathode	8	D_1 Common anode
2	d Cathode	9	D_2 Common anode
3	c Cathode	10	Lower point C
4	b Cathode	11	Point commonanode
5	a Cathode	12	Uppon point C
6	g Cathode	13	D_3 Common anode
7	f Cathode	14	D_4 Common anode

0.3. INCH 4 DIGITS RED OR GREEN LED NUMERIC DISPLAY

GENERAL DESCRIPTION

The MDE 2583...4R and MDE 2583...4V are common cathode seven segment GaP numeric displays. The large 7.62 (0.3 inch) high characters size generate a bright, continously uniform seven segment display. They are made on printed circuit boards and plastic encapsulated.

FEATURES

- High Luminous Intensity
- Wide Viewing Angle
- Uniform Alignement
- IC (TTL) Compatible
- Multiplexed adressable

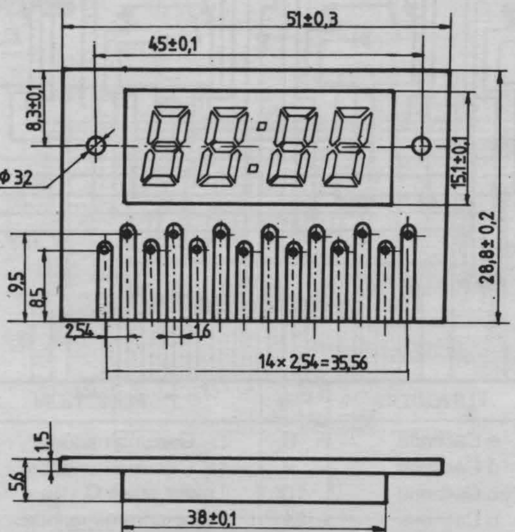
APPLICATIONS

To display digital information used in electrical equipments where it is neccessary.

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	VALUES	UNIT
I_F	DC Forward Current	20	mA/seg
I_{FP}	Pulse (width =1 msec, duty ratio = 25%) Forward Current	60	mA/seg
V_R	Reverse Voltage	3	V
P_D	Power Dissipation	300	mW
T_A	Operating Temperature	−40...+85	°C
T_{stg}	Storage Temperature	−40...+85	°C

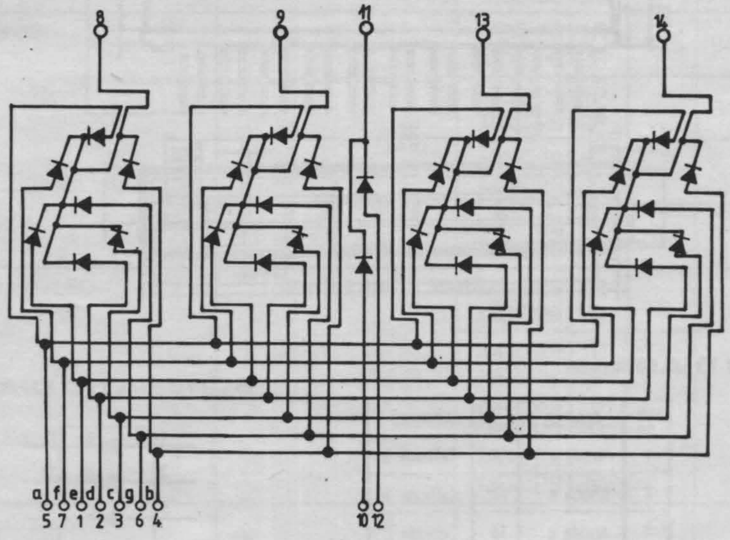
PACKAGE DIMENSIONS



OPTOELECTRIC CHARACTERISTICS AT $T_A = 25°C$

PARAMETER		TEST CONDITIONS	DEVICE	VALUES		UNIT
				Min.	Max.	
V_F	Forward Voltage	$I_F = 10$ mA/seg		1.9	3	V
V_R	Reverse Breakdown Voltage	$I_R = 100$ μA/seg		3		V/seg
I_V	Luminous Intensity	$I_F = 10$ mA/seg	MDE 2583R MDE 2583V	180		μcd/seg
			MDE 2584R MDE 2584V	300		μcd/seg
λ_p	Emission Peak Wavelength	$I_F = 10$ mA/seg	MDE 2583R MDE 2584R	645	725	nm
			MDE 2583V MDE 2584V	554	570	nm
$\Delta\lambda$	Line Half Width	$I_F = 10$ mA/seg			100	nm
Co	Capacitance	$V_F = 0V$ f = 1 MHz			200	pF
t	Response Time			500		nsec

INTERNAL CIRCUIT DIAGRAM



PIN	FUNCTION	PIN	FUNCTION
1	e Anode	8	D_1 Common cathode
2	d Anode	9	D_2 Common cathode
3	c Anode	10	Lower point A
4	b Anode	11	Point commoncathode
5	a Anode	12	Uppon point A
6	g Anode	13	D_3 Common cathode
7	f Anode	14	D_4 Common cathode

LIGHT INDICATOR WITH DISCRET LED S (BAR GRAPH DISPLAY)

GENERAL DESCRIPTION

The MDE 2911...2R (P, G or V) are light indicators with $GaAs_{1-x}P_x$ (x = 0...1) LED s. Discret LEDs are made by planar process and epoxy encapsulated.
The 10 rectangular LED s are finaly encapsulated in a plastic suport.

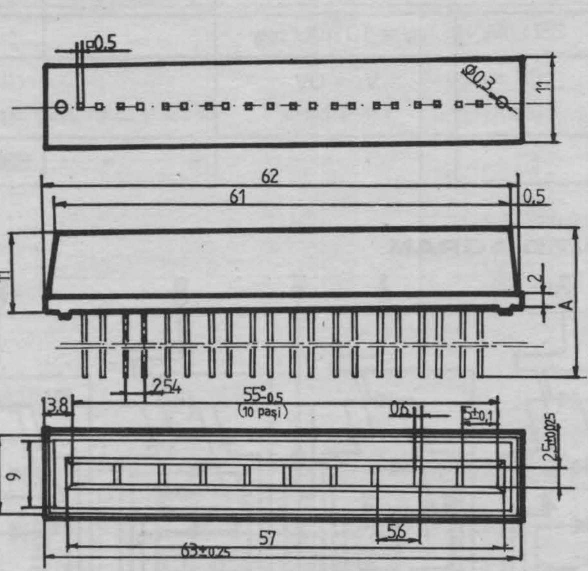
FEATURES

- High Luminous Intensity
- Low Power Requirements
- High Reliability and Long Life
- Light Emitting Uniformity

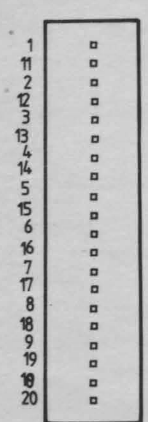
APPLICATIONS

- Illuminated Legends
- Indicators
- Level Meters
- Audio Devices

PACKAGE DIMENSIONS

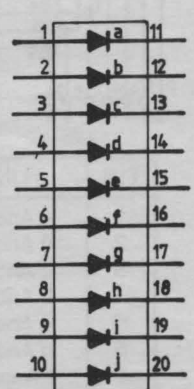


CONNECTION DIAGRAM



PIN no	ADRESS	PIN no	ADRESS
1	Anode a	11	Cathode a
2	Anode b	12	Cathode b
3	Anode c	13	Cathode c
4	Anode d	14	Cathode d
5	Anode e	15	Cathode e
6	Anode f	16	Cathode f
7	Anode g	17	Cathode g
8	Anode h	18	Cathode h
9	Anode i	19	Cathode i
10	Anode j	20	Cathode j

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUES	UNIT
I_{Fmax} DC Forward Current	50	mA
$I_{Fpeak\ max}$ Peak Forward Current per LED (1 μsec. pulse width, 300 pps)	1	A
$P_{d\ max}$ DC Power Dissipation per LED	150	mW
T_A Operating Temperature	0...+70	°C
T_{stg} Storage Temperature	−40...+85	°C
T_{ead} Lead Soldering Temperature	+260	°C

OPTOELECTRONIC CHARACTERISTICS AT $T_A = 25°C$

PARAMETER	TEST CONDITIONS	DEVICE	VALUES Min.	VALUES Max.	UNIT
I_V Luminous Intensity	$I_F = 20$ mA	MDE 2911R MDE 2911P MDE 2911G MDE 2911V	0.1	1	mcd
		MDE 2912R MDE 2912P MDE 2912G MDE 2912V	1		mcd
λ_p Peak Wavelength	$I_F = 20$ mA	MDE 2911R MDE 2912R	645	680	nm
		MDE 2911P MDE 2912P	625	640	nm
		MDE 2911G MDE 2912G	573	590	nm
		MDE 2911V MDE 2912V	554	570	nm
V_F Forward Voltage/LED	$I_F = 20$ mA	MDE 2911R MDE 2912R		2	V
		MDE 2911P MDE 2912P MDE 2911G MDE 2912G MDE 2911V MDE 2912V		3	V
BV_R Reverse Breakdown Voltage/LED	$I_R = 100$ μA		3		V
Co Capacitance/LED	$V_F = 0$ V, f = 1 MHz	MDE 2911R MDE 2912R		70	pF
		MDE 2911P MDE 2912P MDE 2911G MDE 2912G MDE 2911V MDE 2912V		60	pF

CROSS REFERENCE GUIDE

TYPE MICRO-ELECTRONICA	RCA	NATIONAL SEMICOND	SGS-ATES	MOTOROLA	FAIRCHILD	USSR	CZECH	GDR	POLAND	HUNGARY
CMOS 4000 SERIES										
MMC 4001	CD4001	CD4001	HCF4001	MC14001	F4001	K561LE5	MHB4001	V4001		4001BPC
MMC 4002	CD4002	CD4002	HCF4002	MC14002	F4002	K561LE6	MHB4002	—		—
MMC 4011	CD4011	CD4011	HCF4011	MC14011	F4011	K561LA7	MHB4011	V4011		4011BPC
MMC 4012	CD4012	CD4012	HCF4012	MC14012	F4012	K561LA8	MHB4012	V4012		4012BPC
MMC 4013	CD4013	CD4013	HCF4013	MC14013	F4013	K561TM2	MHB4013	V4013		4013BPC
MMC 4015	CD4015	CD4015	HCF4015	MC14015	F4015	K561IR2	MHB4015	V4015		—
MMC 4017	CD4017	CD4017	HCF4017	MC14017	F4017	K561IE8	—	V4017		4017BPC
MMC 4018	CD4018	CD4018	HCF4018	MC14018	F4018	—	—	—		—
MMC 4019	CD4019	CD4019	HCF4019	MC14019	F4019	K561LS2	—	V4019		—
MMC 4020	CD4020	CD4020	HCF4020	MC14020	F4020	K561IE16	MHB4020	—		4020BPC
MMC 4023	CD4023	CD4023	HCF4023	MC14023	F4023	K561LA9	—	V4023		4023BPC
MMC 4024	CD4024	CD4024	HCF4024	MC14024	F4024	K176IE1	MHB4024	—		—
MMC 4025	CD4025	CD4025	HCF4025	MC14025	F4025	K561LE10	—	—		—
MMC 4027	CD4027	CD4027	HCF4027	MC14027	F4027	K561TV1	—	V4027		4027BPC
MMC 4028	CD4028	CD4028	HCF4028	MC14028	F4028	K561ID1	—	V4028		4028BPC
MMC 4029	CD4029	CD4029	HCF4029	MC14029	F4029	—	MHB4029	V4029		4029BPC
MMC 4030	CD4030	CD4030	HCF4030	MC14507	F4030	K561LP2	MHB4030	V4030		4030BPC
MMC 4031	CD4031	CD4031	HCF4031	—	F4031	K176IR4	—	—		—
MMC 4035	CD4035	CD4035	HCF4035	MC14035	F4035	K561IR9	—	V4035		—
MMC 4041	CD4041	CD4041	HCF4041	MC14041	F4041	—	—	—		—
MMC 4042	CD4042	CD4042	HCF4042	MC14042	F4042	K561TM3	—	V4042		4042BPC
MMC 4043	CD4043	CD4043	HCF4043	MC14043	F4043	K561LTR2	—	—		—
MMC 4044	CD4044	CD4044	HCF4044	MC14044	F4044	—	—	V4044		4044BPC
MMC 4047	CD4047	CD4047	HCF4047	—	F4047	—	—	—		—
MMC 4049	CD4049	CD4049	HCF4049	MC14049	F4049	K561LN2	—	—		4049UBPC
MMC 4050	CD4050	CD4050	HCF4050	MC14050	F4050	K561PU4	MHB4050	V4050		4050BPC
MMC 4051	CD4051	CD4051	HCF4051	MC14051	F4051	K561KP2	MHB4051	—		—
MMC 4052	CD4052	CD4052	HCF4052	MC14052	F4052	K561KPI	MHB4052	—		—
MMC 4053	CD4053	CD4053	HCF4053	MC14053	F4053	—	MHB4053	—		—
MMC 4054	CD4054	CD4054	HCF4054	MC14054	F4054	—	—	—		—
MMC 4060	CD4060	CD4060	HCF4060	MC14060	F4060	—	—	—		4060BPC
MMC 4066	CD4066	CD4066	HCF4066	MC14066	F4066	K561KT3	MHB4066	—		4066BPC
MMC 4067	CD4067		HCF4067		F4067	—	—	—		—
MMC 4069	CD4069	CD4069	HCF4069	MC14069	F4069	—	—	—		4069UBPC
MMC 4071	CD4071	CD4071	HCF4071	MC14071	F4071		—	—		4071BPC
MMC 4072	CD4072	CD4072	HCF4072	MC14072	F4072		—	—		—
MMC 4073	CD4073	CD4073	HCF4073	MC14073	F4073		—	—		4073BPC
MMC 4081	CD4081	CD4081	HCF4081	MC14081	F4081		MHB4081	—		4081BPC
MMC 4093	CD4093	CD4093	HCF4093	MC14093	F4093		—	V4093		4093BPC

TYPE MICRO-ELECTRONICA	RCA	NATIONAL SEMICOND.	SGS-ATES	MOTOROLA	FAIRCHILD	USSR	CZECH	GDR	POLAND	HUNGARY
MMC 4097	CD4097		HCF4097	—	—		—	—		—
MMC 4098	CD4098	CD4098	HCF4098	MC14598	F4098		—	—		4098BPC
MMC 40104			HCF40104	—	—		—	—		—
MMC 40107	CD40107		HCF40107	—	—		—	—		—
MMC 40181	CD40181	CD40181	HCF40181	MC14581	F40181		—	—		—
MMC 40192	CD40192	CD40192	HCF40192	MC140192	F40192	—	—	—		—
MMC 4510	CD4510	CD4510	HCF4510	MC14510	F4510		—	—		4510BPC
MMC 4511	CD4511	CD4511	HCF4511	MC14511	F4511		MHB4511			4511BPC
MMC 4516	CD4516	CD4516	HCF4516	MC14516	F4516		—	—		4516BPC
MMC 4518	CD4518	CD4518	HCF4518	MC14518	F4518		MHB4518	—		4518BPC
MMC 4520	CD4520	CD4520	HCF4520	MC14520	F4520	K561IEIO	—	—		—
MMC 4543		CD4543					MHB4543	—		—

RAM MEMORIES

TYPE MICRO-ELECTRONICA	RCA	NATIONAL SEMICOND.	SGS-ATES	MOTOROLA	FAIRCHILD	USSR	CZECH	GDR	POLAND	HUNGARY
MMN 2102		MM2102	M2102	—		K565RU2	MHB2102	U202	MCY7102	2102PC
MMN 2114		MM2114	M2102	MCM2114		—	MHB2114	—	MCY7114	—
MMN 4027		MM5280	M4027	MCM4027						
MMN 4116		MM5290	M4116	MCM4116		K565RU3	MHB4116	U256		4116PC

MMN 8080 MICROPROCESSOR FAMILY

TYPE MICRO-ELECTRONICA	INTEL	NATIONAL SEMICOND.	TEXAS INSTRUMENTS	USSR	POLAND
MMN 8080	8080	INS 8080	TMS 8080	KR580IK80A	MCY7880
MMN 8251	8251	INS 8251	TMS 8251	KR580IK51	MCY7851
MMN 8255	8255	INS 8255	TMS 8255	KR580IK55	MCY7855
MMN 8257	8257	INS 8257	TMS 8257	KR580IK57	
MMN 8205	8205	INS 8205	TMS 8205		UCY74S405
MMN 8214	8214	INS 8214	TMS 8214		UCY74S414
MMN 8216	8216	INS 8216	TMS 8216		UCY74S416
MMN 8224	8224	INS 8224	TMS 8224		UCY74S424
MMN 8226	8226	INS 8226	TMS 8226		UCY74S426
MMN 8228	8228	INS 8228	TMS 8228		UCY74S428
MMN 8238	8238	INS 8238	TMS 8238		—

MMN 80 MICROPROCESSOR FAMILY

TYP MICROELECTRONICA	SGS-ATES	ZILOG
MMN 80 CPU	Z 8400	Z 80 — CPU
MMN 80 SIO	Z 8440/1/2	Z 80 — SIO
MMN 80 CTC	Z 8430	Z 80 — CTC
MMN 80 PIO	Z 8420	Z 80 — PIO
MMN 80 DMA	Z 8410	Z 80 — DMA

ANALOG SWITCHES

TYP MICROELECTRONICA	SILICONIX	INTERSIL	NATIONAL SEMICONDUCTORS
MMP 115	G 115	G 115	MM 5504*
MMP 116	G 116	G 116	—
MMP 117	G 117	G 117	—
MMP 119	G 119	G 119	—
MMP 122	G 122	G 122	MM 550*
MMP 124	G 124	MM 551*	MM 551*

SHIFT REGISTERS

MICROELECTRONICA	PHILIPS MULLARD SIEMENS
MMP 156	FDN 156

PMOS

MICROELECTRONICA	SIEMENS	GDR	MOSTEK
MMP 131	SAJ 131	—	—
MMP 190	S190	—	—
MMP 710	—	U 710	—
MMP 711	—	U 711	—
MMP 5002/5/7			MK 5002
MMP 5009			MK 5009

SPECIAL CMOS

MICROELECTRONICA	ITT	SGS — ATES
MMC 300	SAJ 300	M 730
MMC 760	—	M 760

* functional equivalent

ERRATUM

Page 285:
To the table DECODER INPUT DATA read INPUT DATA not OUTPUT DATA
Page 306:
The characteristics of MDE 1541...3 R, P, G, V same to MDE 1101...3R, P, G, V

All connection diagrams are top view.

Tiparul executat sub comanda nr. 40441 la
Combinatul Poligrafic „Casa Scînteii",
Str. Piața Scînteii Nr. 1 — București
Republica Socialistă România